Microwave Devices and Circuits

Third Edition

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Chapter 6

Microwave Field-Effect Transistors

6-0 INTRODUCTION

After Shockley and his coworkers invented the transistor in 1948, he proposed in 1952 a new type of field-effect transistor (FET) in which the conductivity of a layer of a semiconductor is modulated by a transverse electric field [1]. In a conventional transistor both the majority and the minority carriers are involved; hence this type of transistor is customarily referred to as a *bipolar* transistor. In a field-effect transistor the current flow is carried by majority carriers only; this type is referred to as a *unipolar* transistor. In addition, the field-effect transistors are controlled by a voltage at the third terminal rather than by a current as with bipolar transistors. Our purpose here is to describe the physical structures, principles of operation, microwave characteristics, and power-frequency limitations of unipolar field-effect transistors. Since the microwave field-effect transistor has the capability of amplifying small signals up to the frequency range of X band with low-noise figures, it has lately replaced the parametric amplifier in airborne radar systems because the latter is complicated in fabrication and expensive in production.

The unipolar field-effect transistor has several advantages over the bipolar junction transistor:

1. It may have voltage gain in addition to current gain.
2. Its efficiency is higher than that of a bipolar transistor.
3. Its noise figure is low.
4. Its operating frequency is up to X band.
5. Its input resistance is very high, up to several megohms.

Among the unipolar field-effect transistors are the junction field-effect transistors, metal-semiconductor field-effect transistors, high electron-mobility transistors, and the metal-oxide-semiconductor field-effect transistors. All these devices are analyzed in this chapter.

6-1 JUNCTION FIELD-EFFECT TRANSISTORS (JFETs)

Unipolar field-effect transistors may be in the form of either a p-n junction gate or a Schottky-barrier gate. The former is called a *junction field-effect transistor* (JFET), and the latter is referred to as a MESFET or *metal-semiconductor field-effect transistor*. The JFET was originally proposed by Shockley [1]. Figure 6-1-1 shows the schematic diagram and circuit symbol for an n-channel JFET.

6-1-1 Physical Structure

The n-type material is sandwiched between two highly doped layers of p-type material that is designated P^+. This type of device is called an *n-channel JFET*. If the middle part is a p-type semiconductor, the device is called a *p-channel JFET*. The two p-type regions in the n-channel JFET shown in Fig. 6-1-1 are referred to as the *gates*. Each end of the n channel is joined by a metallic contact. In accordance with the directions of the biasing voltages shown in Fig. 6-1-1, the left-hand contact which supplies the source of the flowing electrons is referred to as the *source*, whereas the right-hand contact which drains the electrons out of the material is called the *drain*. The circuit symbol for an n-channel JFET is also shown in Fig. 6-1-1. The direction of the drain current I_d is flowing from the drain to the device.

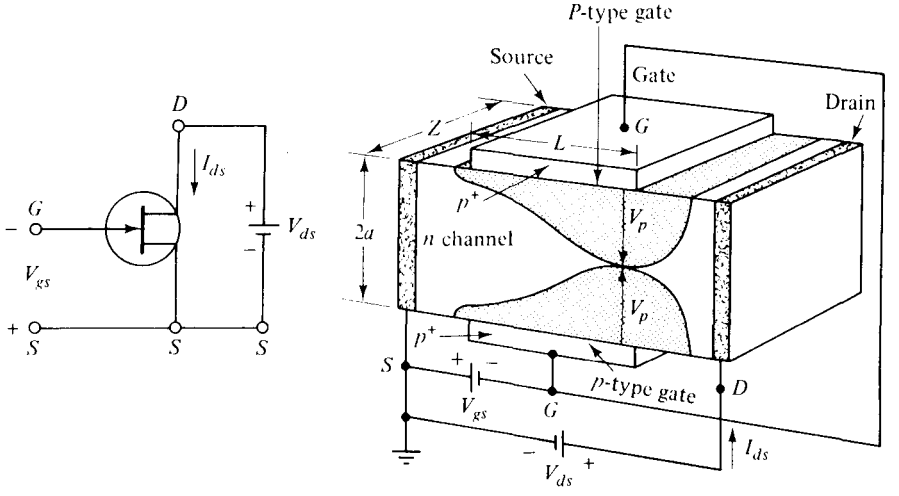


Figure 6-1-1 Schematic diagram and circuit symbol for an n-channel JFET.

For a p-channel JFET, the polarities of the two biasing voltages V_g and V_d are interchanged, the head of the arrow points away from the device, and the drain current I_d flows away from the device. Since electrons have higher mobility than holes, the n-channel JFET provides higher conductivity and higher speed and is preferred in most applications to the p-channel JFET.

6-1-2 Principles of Operation

Under normal operating conditions, when the gate voltage V_g is zero, the drain current I_d is also zero. The channel between the gate junctions is entirely open. When a small drain voltage V_d is applied between the drain and source, the n-type semiconductor bar acts as a simple resistor, and the current I_d increases linearly with V_d. If a reverse gate voltage V_g is applied across the p-n gate junctions, the majority of free electrons are depleted from the channel, and the space-charge regions are extended into the channel. As the drain voltage V_d is further increased, the space-charge regions expand and join together, so that all free electron carriers are completely depleted in the joined region. This condition is called *pinch off*. When the channel is pinched off, the drain current I_d remains almost constant, but the drain voltage V_d is continuously increased.

Pinch-off voltage *Vp*. The pinch-off voltage is the gate reverse voltage that removes all the free charge from the channel. The Poisson's equation for the voltage in the n channel, in terms of the volume charge density is given by

$$\frac{d^2V}{dy^2} = -\frac{\rho}{\epsilon_s} = -\frac{qN_d}{\epsilon_s} = -\frac{qN_d}{\epsilon_r\epsilon_o} \tag{6-1-1}$$

where ρ = volume charge density in coulombs per cubic meter
q = charge in coulombs
N_d = electron concentration in electrons per cubic meter
ϵ_s = permittivity of the material in farads per meter
$\epsilon_s = \epsilon_r\epsilon_o$, ϵ_r is the relative dielectric constant
$\epsilon_o = 8.854 \times 10^{-12}$ F/m is the permittivity of free space

Integration of Eq. (6-1-1) once and application of the boundary condition of the electric field $E = -\dfrac{dV}{dy} = 0$ at $y = a$ yield

$$\frac{dV}{dy} = -\frac{qN_d}{\epsilon_s}(y - a) \qquad \text{volts per meter} \tag{6-1-2}$$

Integration of Eq. (6-1-2) once and application of the boundary condition $V = 0$ at $y = 0$ result in

$$V = -\frac{qN_d}{2\epsilon_s}(y^2 - 2ay) \qquad \text{volts} \tag{6-1-3}$$

Then the pinch-off voltage V_p at $y = a$ is expressed as

$$V_p = \frac{qN_d a^2}{2\epsilon_s} \quad \text{volts} \tag{6-1-4}$$

where a is the height of the channel in meters.

Equation (6-1-4) indicates that the pinch-off voltage is a function of the doping concentration N_d and the channel height a. Doping may be increased to the limit set by the gate breakdown voltage, and the pinch-off voltage may be made large enough so that drift-saturation effects just become dominant.

From Fig. 6-1-1, the pinch-off voltage under saturation condition can be expressed as

$$V_p = V_d + |V_g| + \psi_o \tag{6-1-5}$$

where $|V_g|$ = absolute value of the gate voltage
ψ_o = built-in or barrier voltage at the junction

The saturation drain voltage is then given by

$$V_{d\,\text{sat}} = \frac{qN_d a^2}{2\epsilon_s} - |V_g| - \psi_o \tag{6-1-6}$$

The JFET has a conducting channel between the source and the drain electrodes when the gate bias voltage is zero. This is the ON state, and the transistor is called a *normally* ON *JFET*. In order to reach the OFF state, a gate voltage must be applied to deplete all carriers in the channel. As a result, this device is referred to as the *depletion-mode JFET* or *D-JFET*.

Example 6-1-1: Pinch-Off Voltage of a Silicon JFET

A certain Si JFET has the following parameters:

Channel height:	$a = 0.1\ \mu\text{m}$
Electron concentration:	$N_d = 8 \times 10^{17}\ \text{cm}^{-3}$
Relative dielectric constant:	$\epsilon_r = 11.80$

Calculate the pinch-off voltage.

Solution From Eq. (6-1-6), the pinch-off voltage is

$$V_p = \frac{qN_d a^2}{2\epsilon_s} = \frac{1.6 \times 10^{-19} \times 8 \times 10^{23} \times (0.1 \times 10^{-6})^2}{2 \times 8.854 \times 10^{-12} \times 11.8}$$

$$= 6.66 \text{ volts}$$

6-1-3 Current-Voltage (I-V) Characteristics

The drain current of an n-channel JFET is dependent on the drain and gate voltages and the channel resistance. The n-channel resistance can be expressed as

$$R = \frac{\rho L}{A} = \frac{L}{\sigma A} = \frac{L}{q\mu_n N_d A} = \frac{L}{2q\mu_n N_d Z(a - W)} \tag{6-1-7}$$

where μ_n = electron mobility
Z = distance in z direction
L = length in x direction
W = depletion-layer width
a = width between two p-n junctions

The drain voltage across an elemental section dx of the channel is given by

$$dV(x) = I_d dR = \frac{I_d dx}{2q\mu_n N_d Z[a - W(x)]} \tag{6-1-8}$$

From Eq. (6-1-6), the depletion-layer width can be written as

$$W(x) = \left[\frac{2\epsilon_s[V(x) + |V_g| + \psi_o]}{qN_d}\right]^{1/2} \tag{6-1-9}$$

Then

$$Wdw = \frac{\epsilon_s}{qN_d} dV \tag{6-1-10}$$

The drain current I_d is expressed by

$$I_d = 2q\mu_n N_d Z[a - W(x)]\frac{dV}{dx} \tag{6-1-11}$$

Substituting Eq. (6-1-10) into Eq. (6-1-11) and integrating from $x = 0$ to $x = L$ give the drain current as

$$\begin{aligned} I_d &= \frac{2q^2\mu_n N_d^2 Z}{L\epsilon_s}\int_{w_1}^{w_2}(a - W)Wdw \\ &= \frac{\mu_n q^2 N_d^2 Z}{L\epsilon_s}\left[a(W_2^2 - W_1^2) - \frac{2}{3}(W_2^3 - W_1^3)\right] \end{aligned} \tag{6-1-12}$$

Boundary conditions. The channel-to-gate voltage can be written from Eq. (6-1-4) as

$$V_{cg} = \frac{qN_d W^2}{2\epsilon_s} = \frac{qN_d a^2 W^2}{2\epsilon_s a^2} = V_p\frac{W^2}{a^2} = V(x) + |V_g| + \psi_o \tag{6-1-13}$$

The depletion-layer width is

$$W = a\left(\frac{V(x) + |V_g| + \psi_o}{V_p}\right)^{1/2} \tag{6-1-14}$$

Then

$$W_1^2 = a^2\left(\frac{|V_g| + \psi_o}{V_p}\right) \qquad \text{at } x = 0 \text{ and } V(x) = 0 \tag{6-1-15}$$

and

$$W_2^2 = a^2\left(\frac{V_d + |V_g| + \psi_o}{V_p}\right) \qquad \text{at } x = L \text{ and } V(x) = V_d \tag{6-1-16}$$

Substituting Eqs. (6-1-15) and (6-1-16) into Eq. (6-1-12) yields the drain current

$$I_d = I_p\left[\frac{V_d}{V_p} - \frac{2}{3}\left(\frac{V_d + |V_g| + \psi_o}{V_p}\right)^{3/2} + \frac{2}{3}\left(\frac{|V_g| + \psi_o}{V_p}\right)^{3/2}\right] \tag{6-1-17}$$

where $I_p = \dfrac{\mu_n q^2 N_d^2 Z a^3}{L\epsilon_s}$ is the pinch-off current.

Figure 6-1-2 shows the normalized ideal current-voltage characteristics for a pinch-off voltage of 3.2 volts [1].

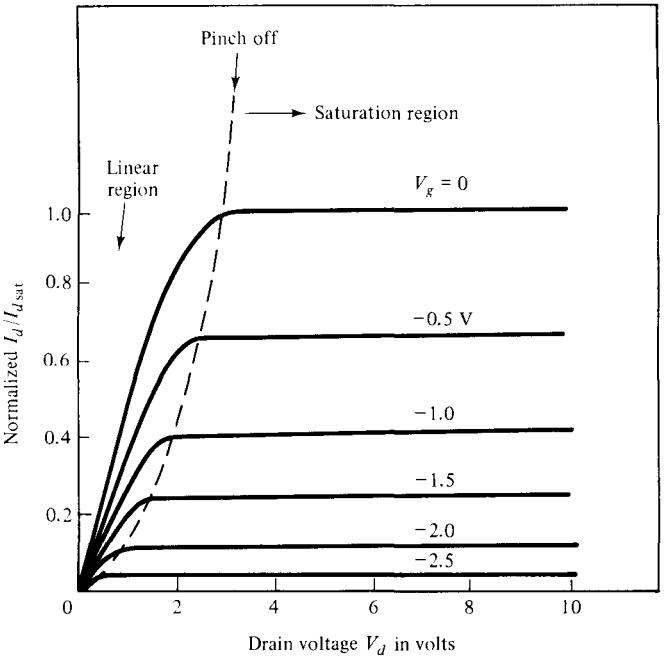


Figure 6-1-2 Normalized ideal *I-V* characteristics of a typical JFET.

Linear region. In the linear region at $V_d \ll (|V_g| + \psi_o)$, the drain current can be expressed from Eq. (6-1-12) as

$$I_d = \frac{I_p V_d}{V_p}\left[1 - \left(\frac{|V_g| + \psi_o}{V_p}\right)^{1/2}\right] \tag{6-1-18}$$

The channel conductance (or the drain conductance) is given by

$$g_d = \left.\frac{\partial I_d}{\partial V_d}\right|_{V_g=\text{constant}} = \frac{I_p}{V_p}\left[1 - \left(\frac{|V_g| + \psi_o}{V_p}\right)^{1/2}\right] \tag{6-1-19}$$

The mutual conductance (or transconductance) is expressed as

$$g_m = \left.\frac{\partial I_d}{\partial V_g}\right|_{V_d=\text{constant}} = \frac{I_p V_d}{2V_p^2}\left[1 - \left(\frac{V_p}{|V_g| + \psi_o}\right)^{1/2}\right] \tag{6-1-20}$$

Saturation region. At the pinch-off voltage, the drain current becomes saturated. By setting $V_p = V_d + |V_g| + \psi_o$, the saturation drain current is given by

$$I_{d\,\text{sat}} = I_p\left[\frac{1}{3} - \left(\frac{|V_g| + \psi_o}{V_p}\right) + \frac{2}{3}\left(\frac{|V_g| + \psi_o}{V_p}\right)^{3/2}\right] \tag{6-1-21}$$

and the corresponding saturation drain voltage as

$$V_{d\,\text{sat}} = V_p + |V_g| + \psi_o \tag{6-1-22}$$

The mutual conductance in the saturation region is then expressed as

$$g_m = \frac{\partial I_d}{\partial V_g}\bigg|_{V_d=\text{constant}} = \frac{I_p}{V_p}\left[1 - \left(\frac{|V_g| + \psi_o}{V_p}\right)^{1/2}\right] \tag{6-1-23}$$

where $\dfrac{I_p}{V_p} = \dfrac{2\mu_n q N_d a Z}{L}$

It should be noted that the g_m in the saturation region is identical to the one in the linear region.

For a small signal, the drain or output resistance is defined as

$$r_d = \frac{\partial V_d}{\partial I_d}\bigg|_{V_g=\text{constant}} \tag{6-1-24}$$

Then the amplification factor for a JFET may be defined as

$$\mu = \frac{\partial V_d}{\partial V_g}\bigg|_{I_d=\text{constant}} = r_d g_m \tag{6-1-25}$$

The cutoff frequency is given by

$$f_c = \frac{g_m}{2\pi C_g} = \frac{I_p/V_p}{2\pi Z L \epsilon_s/(2a)} = \frac{2\mu_n q N_d a^2}{\pi \epsilon_s L^2} \tag{6-1-26}$$

where $C_g = \dfrac{LZ\epsilon_s}{2a}$ is the capacitance between gate and source

Pinch-off region. When an electric field appears along the x axis between the drain and the source, the drain end of the gate is more reverse-biased than the source end. Hence the boundaries of the depletion region are not parallel to the center of the channel, but converged as shown in Fig. 6-1-2. As the drain voltage V_d and drain current I_d are further increased, the channel is finally pinched off.

Breakdown voltage. As the drain voltage V_d increases for a constant gate voltage V_g, the bias-voltage causes avalanche breakdown across the gate junction, and the drain current I_d increases sharply. The breakdown voltage is shown in Fig. 6-1-3 by the relationship

$$V_b = V_d + |V_g|$$

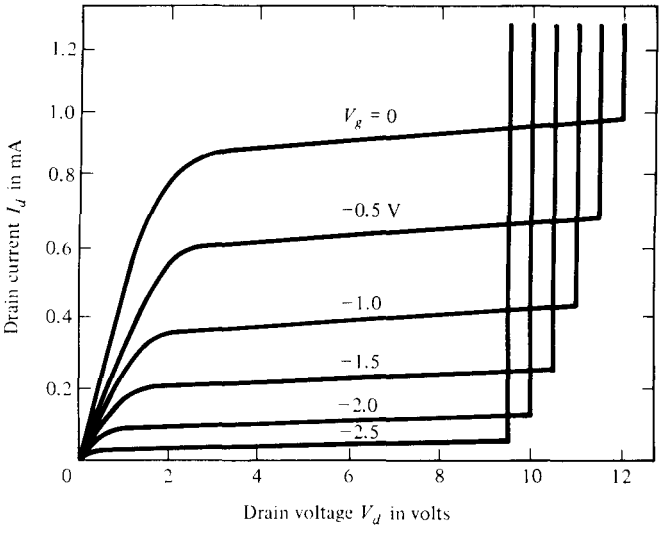


Figure 6-1-3 Breakdown voltage for a typical JFET.

Example 6-1-2: Current of a JFET

A silicon JFET at 300° K has the following parameters:

Electron density:	$N_d = 1 \times 10^{17}\ \text{cm}^{-3}$
Hole density:	$N_a = 1 \times 10^{19}\ \text{cm}^{-3}$
Relative dielectric constant:	$\epsilon_r = 11.8$
Channel height:	$a = 0.2 \times 10^{-4}\ \text{cm}$
Channel length:	$L = 8 \times 10^{-4}\ \text{cm}$
Channel width:	$Z = 50 \times 10^{-4}\ \text{cm}$
Electron mobility:	$\mu_n = 800\ \text{cm}^2/\text{V}\cdot\text{s}$
Drain voltage:	$V_d = 10\text{V}$
Gate voltage:	$V_g = -1.5\ \text{V}$

Compute:

a. The pinch-off voltage in volts
b. The pinch-off current in mA
c. The built-in voltage in V
d. The drain current in mA
e. The saturation drain current at $V_g = 0$
f. The cutoff frequency

Solution

a. The pinch-off voltage is

$$V_p = \frac{1.6 \times 10^{-19} \times 1 \times 10^{17} \times (0.2 \times 10^{-4})^2}{2 \times 8.854 \times 10^{-14} \times 11.8} = 3.06\ \text{V}$$

b. The pinch-off current is

$$I_p = \frac{800 \times (1.6 \times 10^{-19})^2 (1 \times 10^{17})^2 (50 \times 10^{-4})(0.2 \times 10^{-4})^3}{8 \times 10^{-4} \times 8.854 \times 10^{-14} \times 11.8}$$

$$= 9.80 \text{ mA}$$

c. The built-in voltage is

$$\psi_o = 26 \times 10^{-3} \ln\left[\frac{1 \times 10^{17} \times 1 \times 10^{19}}{(1.5 \times 10^{10})^2}\right] = 0.936 \text{ V}$$

d. The drain current is computed from Eq. (6-1-17) as

$$I_d = 9.8 \times 10^{-3}\left[\frac{10}{3.06} - \frac{2}{3}\left(\frac{10 + 1.5 + 0.936}{3.06}\right)^{3/2} + \frac{2}{3}\left(\frac{1.5 + 0.936}{3.06}\right)^{3/2}\right]$$

$$= 6.80 \text{ mA}$$

e. The saturation drain current is computed from Eq. (6-1-21) to be

$$I_{d\,\text{sat}} = 6.8 \times 10^{-3}\left[\frac{1}{3} - \left(\frac{1.5 + 0.936}{3.06}\right) + \frac{2}{3}\left(\frac{1.5 + 0.936}{3.06}\right)^{3/2}\right]$$

$$= 0.088 \text{ mA}$$

f. The cutoff frequency is computed from Eq. (6-1-26) as

$$f_c = \frac{2 \times 800 \times 1.6 \times 10^{-19} \times 1 \times 10^{17} \times (0.2 \times 10^{-4})^2}{3.1416 \times 8.854 \times 10^{-14} \times 11.8 \times (8 \times 10^{-4})^2}$$

$$= 4.8 \text{ GHz}$$

The operating frequency must be less than 4.8 GHz.

6-2 METAL-SEMICONDUCTOR FIELD-EFFECT TRANSISTORS (MESFETs)

In 1938, Schottky suggested that the potential barrier could arise from stable space charges in the semiconductor alone without the presence of a chemical layer [2]. The model derived from his theory is known as the *Schottky barrier*.

If the field-effect transistor is constructed with a metal-semiconductor Schottky-barrier diode, the device is called a *metal-semiconductor field-effect transistor* (MESFET). The material may be either silicon or gallium arsenide (GaAs), and the channel type may be either *n* channel or *p* channel.

Since GaAs MEFSETs have the capability of amplifying small signals up to the frequence range of X band with low-noise figure, they have lately replaced the parametric amplifiers in airborne radar systems because the latters are complicated to fabricate and expensive to produce.

The GaAs MESFET has higher electron mobility, higher electric field, and higher electron saturation drift velocity than silicon devices, so its output power is also greater. Another special feature is its lower noise figure, accounted for by its

higher electron mobility. Therefore the GaAs MESFETs are very commonly used in microwave integrated circuits for high-power, low-noise, and broadband amplifier applications.

6-2-1 Physical Structures

The MESFET was developed by many scientists and engineers, such as Mead [3] and Hooper [4], and it is sometimes also called the *Schottky-barrier field-effect transistor*.

The unipolar transistor such as a GaAs MESFET can be developed by using either the epitaxial process or the ion implantation method and those methods are discussed in Chapter 12. Figure 6-2-1 shows schematically a simple MESFET in GaAs.

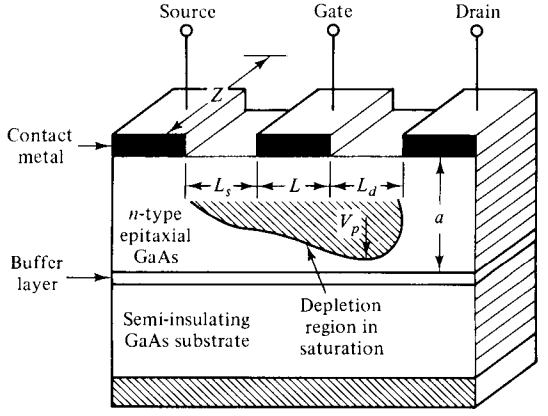


Figure 6-2-1 Schematic diagram of a GaAs MESFET.

In GaAs MESFETs the substrate is doped with chromium (Cr), which has an energy level near the center of the GaAs bandgap. As Cr is the dominant impurity, the Fermi level is pinned near the center of the bandgap. Thus, a very high-resistivity substrate (near 10^8 ohm-cm) generally results, and it is commonly called the *semi-insulator GaAs substrate*. On this nonconducting substrate a thin layer of lightly doped n-type GaAs is grown epitaxially to form the channel region of the field-effect transistor. In many cases a high resistivity GaAs epitaxial layer, called the *buffer layer*, is grown between the n-type GaAs layer and the substrate. The photolithographic process may be used to define the patterns in the metal layers such as Au–Ge for source and drain ohmic contacts and in the Al layer for the Schottky barrier-gate contact. The reason for using GaAs instead of Si is that GaAs has higher electron mobility and can operate at higher temperature and higher power.

The GaAs MESFET can also be grown by using ion implantation. A thin n-type layer can be formed at the surface of the substrate by implanting Si or a donor impurity Se from column VI of the element periodic table. However, the ion implantation process requires an anneal to remove the radiation damage. In either the fully implanted device or the epitaxial device, the source and drain contacts may be improved by further n^+ implantation in these regions.

After the fabrication processes are completed, the individual transistor is separated from the wafer, and this discrete transistor is called a *chip device*. The chip device is then alloyed to a header to provide a contact to the collector region, and Au or Al wires are bonded to the metallized regions to serve as leads to the emitter and base. This bonded chip device is then named a *package transistor*. Figure 6-2-2 shows both the package and chip GaAs MESFET devices.

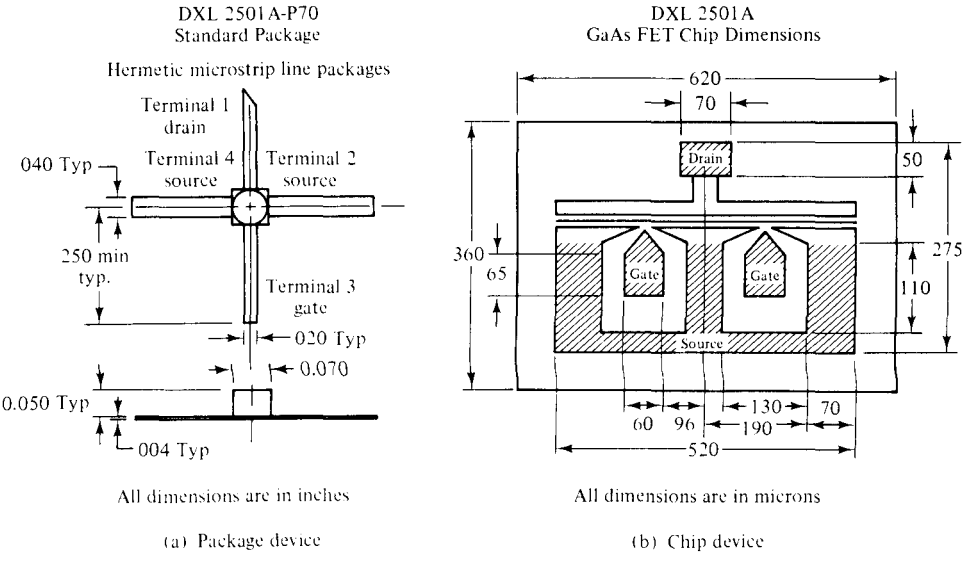


Figure 6-2-2 Dimensions of package and chip GaAs MESFETs.

The MESFET device is of an interdigitated structure, fabricated by using an n-type GaAs epitaxial film about 0.15- to 0.35-μm thick on a semi-insulating substrate about 100 μ. The n-channel layer is doped with either sulphur or tin in a doping concentration N between $8 \times 10^{16}/\text{cm}^3$ and $2 \times 10^{17}/\text{cm}^3$. The electron mobility in the layer is in the range of 3000 to 4500 $\text{cm}^2/\text{V}\cdot\text{s}$. The Schottky barrier-gate is evaporated aluminum. The source and drain contacts are Au–Ge, Au–Te, or Au–Te–Ge alloys. A contact metallization pattern of gold is used to bring the source, drain, and gate contacts out to bonding pads over the semi-insulating substrate. A buffer layer of about 3 μm with a doping concentration of 10^{15} to 10^{16} cm^{-3} is often fabricated between the active n-type epitaxial layer and the semi-insulating substrate.

6-2-2 Principles of Operation

In Fig. 6-2-3 and in Fig. 6-1-1 for JFET, a voltage is applied in the direction to reverse-bias the p-n junction between the source and the gate, while the source and the drain electrodes are forward-biased. Under this bias condition, the majority carriers (electrons) flow in the n-type epitaxial layer from the source electrode, through the channel beneath the gate, to the drain electrode. The current in the channel

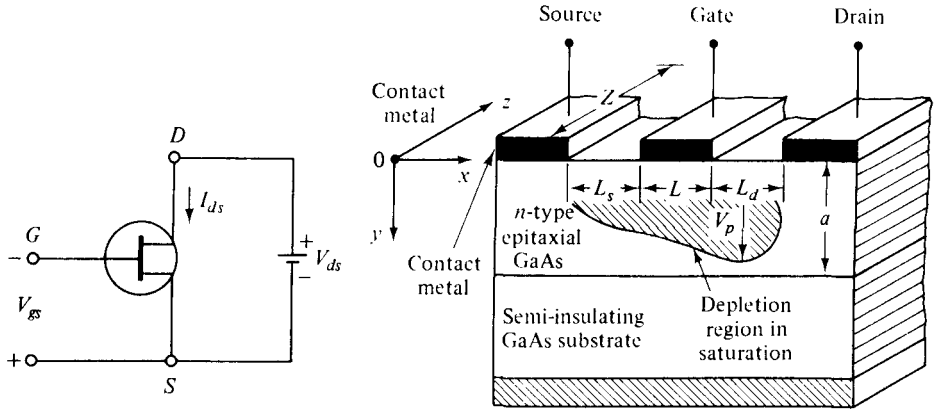


Figure 6-2-3 Schematic diagram and circuit symbol of a GaAs MESFET.

causes a voltage drop along its length so that the Schottky barrier-gate electrode becomes progressively more reverse-biased toward the drain electrode. As a result, a charge-depletion region is set up in the channel and gradually pinches off the channel against the semi-insulating substrate toward the drain end. As the reverse bias between the source and the gate increases, so does the height of the charge-depletion region. The decrease of the channel height in the nonpinched-off region will increase the channel resistance. Consequently, the drain current I_d will be modulated by the gate voltage V_g. This phenomenon is analogous to the characteristics of the collector current I_c versus the collector voltage V_c with the base current I_b as a parameter in a bipolar transistor. In other words, a family of curves of the drain current I_d versus the voltage V_{ds} between the source and drain with the gate voltage V_g as a parameter will be generated in an unipolar GaAs MESFET, as shown in Figure 6-2-4.

The transconductance of a field-effect transistor (FET) is expressed as

$$g_m = \left.\frac{dI_d}{dV_g}\right|_{V_d=\text{constant}} \quad \text{mhos} \tag{6-2-1}$$

For a fixed drain-to-source voltage V_{ds}, the drain current I_d is a function of the reverse-biasing gate voltage V_g. Because the drain current I_d is controlled by the field effect of the gate voltage V_g, this device is referred to as the field-effect transistor. When the drain current I_d is continuously increasing, the ohmic voltage drop between the source and the channel reverse-biases the p-n junction further. As a result, the channel is eventually pinched off. When the channel is pinched off, the drain current I_d will remain almost constant even though the drain-to-source voltage V_d is continuously increased.

Pinch-off voltage V_p. The pinch-off voltage is the gate reverse voltage that removes all the free charge from the channel. Poisson's equation for the voltage in the n channel, in terms of the volume charge density is given by

$$\frac{d^2V}{dy^2} = -\frac{\rho}{\epsilon_s} = -\frac{qN_d}{\epsilon_s} = -\frac{qN_d}{\epsilon_r\epsilon_o} \tag{6-2-2}$$

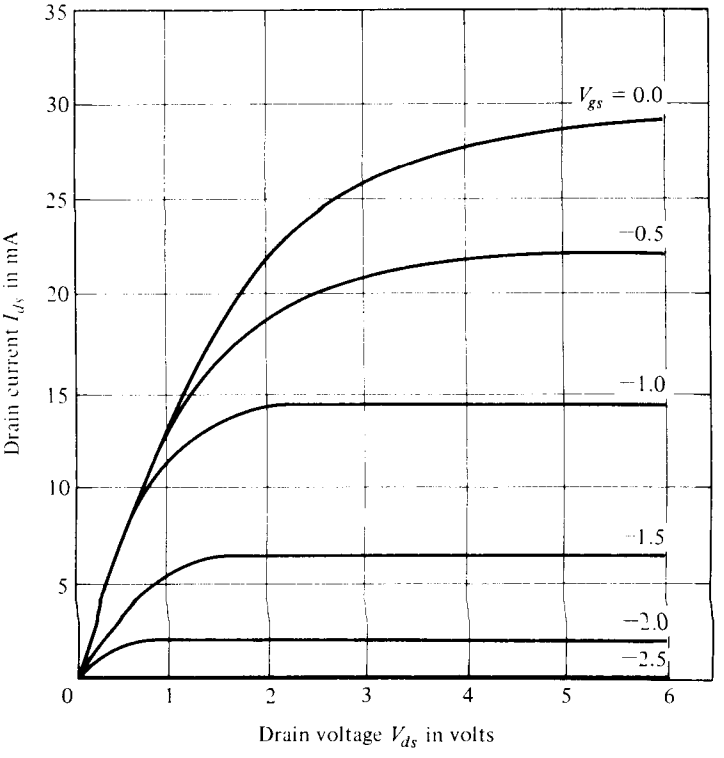


Figure 6-2-4 Current-voltage characteristics of a typical n-channel GaAs MESFET.

where ρ = volume charge density in coulombs per cubic meter
q = charge in coulombs
N_d = electron concentration in electrons per cubic meter
ϵ_s = permittivity of the material in farads per meter
$\epsilon_s = \epsilon_r \epsilon_o$, ϵ_r is the relative dielectric constant
$\epsilon_o = 8.854 \times 10^{-12}$ F/m is the permittivity of free space

Integration of Eq. (6-2-2) twice and application of the boundary condition yield the pinch-off voltage at $y = a$ as

$$V_p = \frac{qN_d a^2}{2\epsilon_s} \quad \text{volts} \tag{6-2-3}$$

where a is the height of the channel in meters.

Equation (6-2-3) indicates that the pinch-off voltage is a function of the doping concentration N_d and the channel height a. Doping may be increased to the limit set by the gate breakdown voltage, and the pinch-off voltage may be made large enough so that drift saturation effects just become dominant.

Example 6-2-1: Pinch-Off Voltage of a MESFET

A certain GaAs MESFET has the following parameters:

Channel height:	$a = 0.1\ \mu\text{m}$
Electron concentration:	$N_d = 8 \times 10^{17}\ \text{cm}^{-3}$
Relative dielectric constant:	$\epsilon_r = 13.10$

Calculate the pinch-off voltage.

Solution From Eq. (6-2-3) the pinch-off voltage is

$$V_p = \frac{qN_d a^2}{2\epsilon_s} = \frac{1.6 \times 10^{-19} \times 8 \times 10^{23} \times (0.1 \times 10^{-6})^2}{2 \times 8.854 \times 10^{-12} \times 13.10}$$

$$= 6.00 \text{ volts}$$

6-2-3 Small-Signal Equivalent Circuit

For microwave frequencies, the metal-semiconductor field-effect transistor (MESFET) has a very short channel length, and its velocity saturation occurs in the channel before reaching the pinched path. The electronic characteristics of a MESFET depend not only on the intrinsic parameters, such as g_m, G_d, R_i, C_{gs}, and C_{gd}, but also on the extrinsic parameters R_g, R_s, C_{ds}, R_p and C_p. Figure 6-2-5 shows the cross section of a MESFET and its equivalent circuit.

The microwave properties of metal-semiconductor field-effect transistors were investigated and analyzed by many scientists and engineers. The noise behavior of these transistors at microwave frequencies has been investigated and measured by van der Ziel and others [5].

1. Intrinsic elements:

g_m = transconductance of the MESFET

G_d = drain conductance

R_i = input resistance

C_{gs} = gate-source capacitance

C_{gd} = gate-drain (or feedback) capacitance

2. Extrinsic elements:

R_g = gate metallization resistance

R_s = source-gate resistance

C_{ds} = drain-source capacitance

R_p = gate bonding-pad parasitic resistance

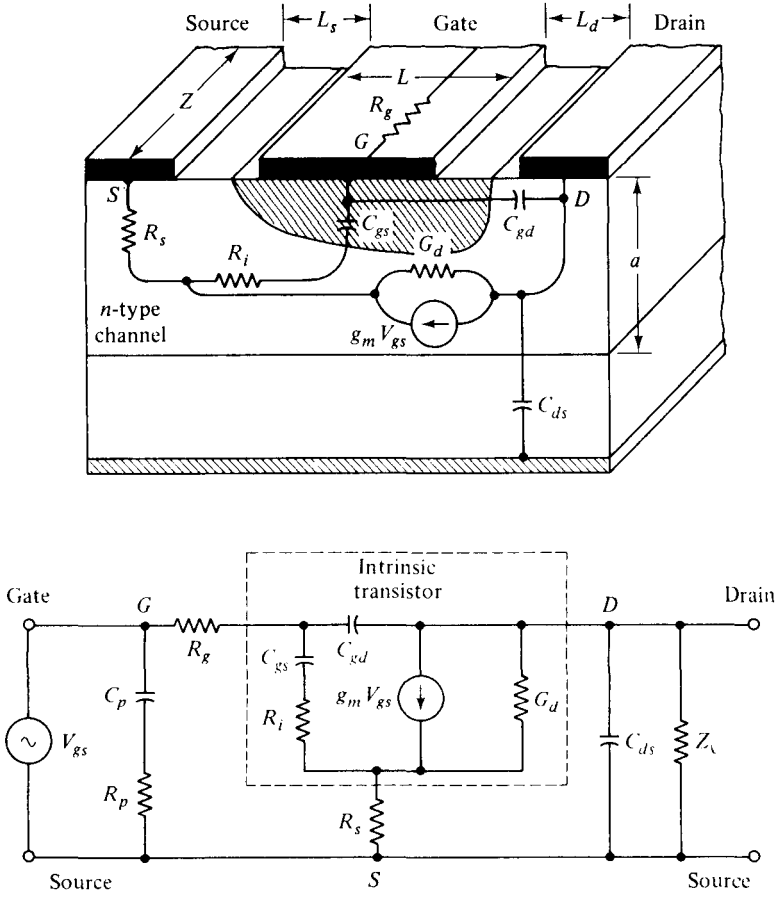


Figure 6-2-5 Cross section and equivalent circuit of a MESFET.

C_p = gate bonding-pad parasitic capacitance

Z_ℓ = load impedance

The values of these intrinsic and extrinsic elements depend on the channel type, material, structure, and dimensions of the Schottky barrier-gate FET. The large values of the extrinsic resistances will seriously decrease the power gain and efficiency and increase the noise figure of the MESFET. It is advantageous to increase the channel doping N as high as possible in order to decrease the relative influence of the feedback capacitance C_{gd} and to increase the transconductance g_m and the dc open-circuit voltage gain. However, an increase in concentration N decreases the breakdown voltage of the gate. A doping of 10^{18} per cubic centimeter might be an upper limit.

6-2-4 Drain Current I_d

The drain current I_d of a Schottky barrier-gate FET is expressed [6] as

$$I_d = I_p \frac{3(\mu^2 - \rho^2) - 2(\mu^3 - \rho^3)}{1 + \eta(\mu^2 - \rho^2)} \quad \text{amperes} \tag{6-2-4}$$

where $I_p = \dfrac{qN_d\mu aZV_p}{3L}$ is the saturation current for the Shockley case at $V_g = 0$

μ = low-field mobility in square meters per volt-second

$q = 1.6 \times 10^{-19}$ coulomb is the electron charge

N_d = doping concentration in electrons per cubic meter

a = channel height

Z = channel depth or width

L = gate length

V_p = pinch-off voltage as defined in Eq. (6-2-3)

$u = \left(\dfrac{V_d + |V_g|}{V_p}\right)^{1/2}$ is the normalized sum of the drain and gate voltages with respect to the pinch-off voltage

$\rho = \left(\dfrac{|V_g|}{V_p}\right)^{1/2}$ is the normalized gate voltage with respect to the pinch-off voltage

$\eta = \dfrac{\mu|V_p|}{v_s L} = \dfrac{v}{v_s}$ is the normalized drift velocity with respect to the saturation drift velocity

v_s = saturation drift velocity

$v = \dfrac{\mu E_x}{1 + \dfrac{\mu E_x}{v_s}}$ is the drift velocity in the channel

E_x = absolute value of the electric field in the channel

Figure 6-2-4 shows a plot of the drain current I_d versus the drain voltage V_{ds} with the gate voltage V_{gs} as a parameter for a typical n-channel GaAs MESFET. The drain current has a maximum at $u = u_m$ given by

$$u_m^3 + 3u_m\left(\frac{1}{z} - \rho^2\right) + 2\rho^3 - \frac{3}{z} = 0 \tag{6-2-5}$$

where $z = \mu|V_p|/(v_s L)$ is the ratio between the small-field velocity extrapolated linearly to the field V_p/L and the saturation velocity

Substitution of Eq. (6-2-5) into Eq. (6-2-4) yields the saturation drain current as

$$I_{d(\text{sat})} = 3I_{dss}(1 - u_m)/z \tag{6-2-6}$$

The transconductance in the saturation region is given by

$$g_m = \left.\frac{\partial I_{d\,\text{sat}}}{\partial|V_g|}\right|_{V_d = \text{constant}} = \frac{g_{\max}(u_m - \rho)}{1 + z(u_m^2 - \rho^2)} \tag{6-2-7}$$

In practice, the drain current and mutual conductance of a GaAs MESFET can be expressed by

$$I_{ds} = I_{dss}\left(1 + \frac{|V_g|}{V_p}\right)^2 \tag{6-2-8}$$

and

$$g_m = \frac{2I_{dss}}{|V_p|}\left(1 + \frac{|V_g|}{V_p}\right) \tag{6-2-9}$$

The velocity-field curves of a GaAs MESFET are very complicated. Figure 6-2-6 shows these curves in the saturation region [7]. The narrowest channel cross section is located under the drain end of the gate. The peak electric field appears near the drain. The drift velocity rises to a peak at x_1, close to the center of the channel, and falls to the low saturated value under the gate edge. To preserve current continuity, heavy electron accumulation has to form in this region because the channel cross section is narrowing. In addition, the electrons are moving progressively slower with increasing x. Exactly the opposite occurs between x_2 and x_3. The channel widens and the electrons move faster, causing a strong depletion layer. The charges in the accumulation and depletion layers are nearly equal, and most of the drain voltage drops in this stationary dipole-layer.

For a Si MESFET, the drain current is expressed as [7]

$$I_d = Zqn(x)v(x)d(x) \tag{6-2-10}$$

where Z = channel depth or width
$n(x)$ = N_d is the density of conduction electrons
$v(x)$ = drift velocity
$d(x)$ = conductive layer thickness
x = coordinate in the direction of the electron drift

The current-voltage characteristics of a Si MESFET are shown in Fig. 6-2-7 [7]. In Fig. 6-2-7(a), there is no metal gate electrode. At the surface of the conducting layer, the source and drain contacts are made. When a positive voltage V_{ds} is applied to the drain, electrons will flow from source to drain. In Fig. 6-2-7(b), a metal gate is added and shorted to the source. When a small drain voltage is applied, a depletion layer is created. The current I_{ds} flowing from drain to source is indicated by Eq. 6-2-7. When the drain voltage V_{ds} is increased, the depletion layer becomes wider. The resulting decrease in conductive cross section d must be compensated by an increase of electron velocity v to maintain a constant current through the channel. As the drain voltage is increased further, the electrons reach their saturation velocity v_s

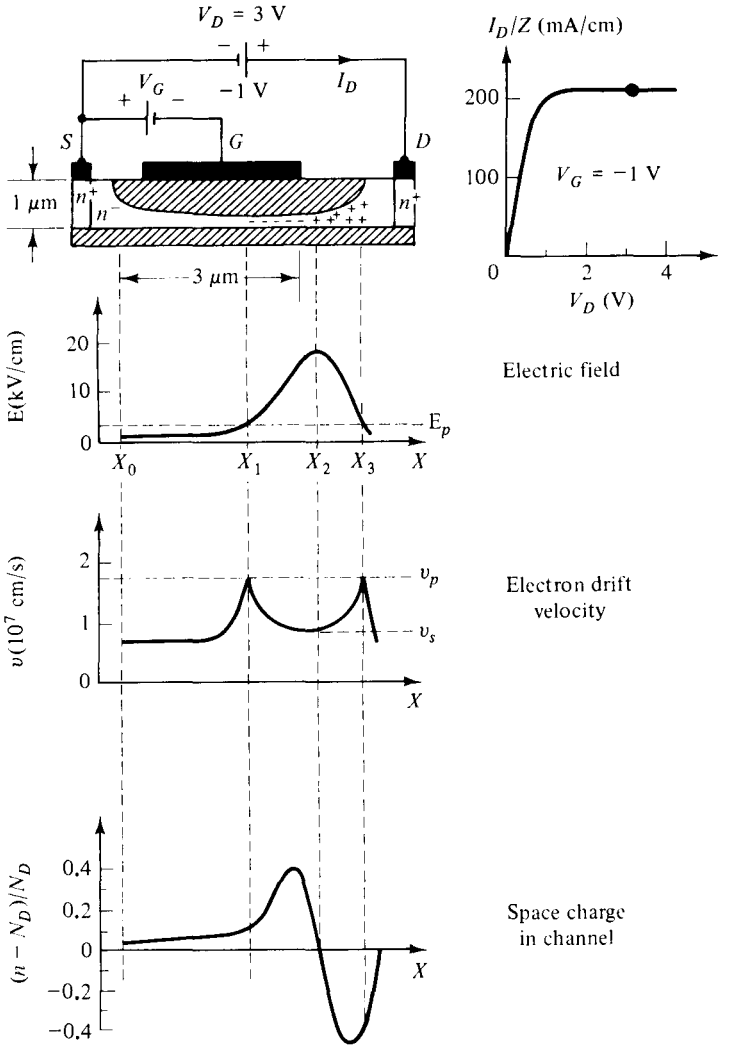


Figure 6-2-6 Channel cross section, electric field, drift velocity, and space charge distribution in the channel of a GaAs MESFET in the saturation region.

as shown in Fig. 6-2-7(c). When the drain voltage is increased beyond $V_{d\,\text{sat}}$, the depletion layer widens toward the drain as indicated in Fig. 6-2-7(d). When a negative voltage is applied to the gate as shown in Fig. 6-2-7(e), the gate-to-channel junction is reverse-biased, and the depletion layer becomes wider. As the gate voltage V_{gs} is more negative, the channel is almost pinched off as shown in Fig. 6-2-7(f), and the drain current I_{ds} is nearly cut off.

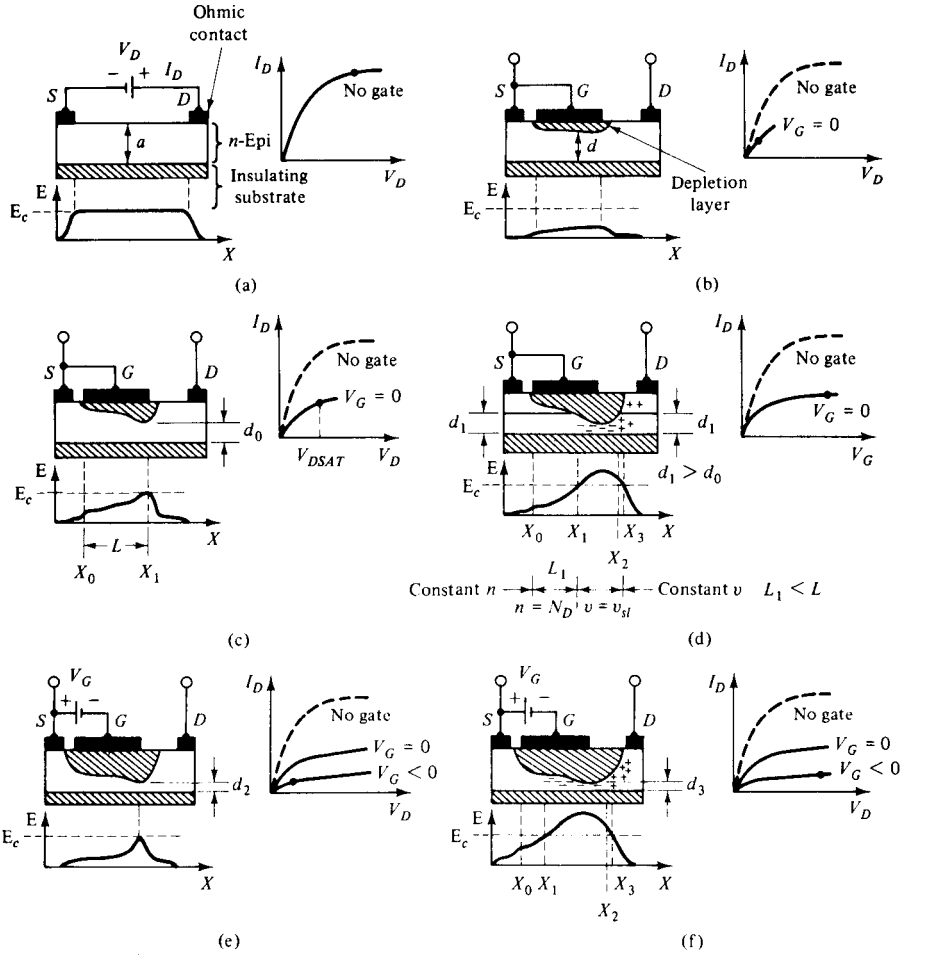


Figure 6-2-7 Electric-field diagrams and current-voltage characteristics of a Si MESFET.

Example 6-2-2: Current-Voltage (*I-V*) Characteristics of a GaAs MESFET

A typical *n*-channel GaAs MESFET has the following parameters:

Electron concentration:	$N_d = 8 \times 10^{17}$ cm^{-3}
Channel height:	$a = 0.1$ μm
Relative dielectric constant:	$\epsilon_r = 13.1$
Channel length:	$L = 14$ μm
Channel width:	$Z = 36$ μm
Electron mobility:	$\mu = 0.08$ m^2/V·s
	$= 800$ cm^2/V·s

Drain voltage: $V_d = 5$ volts
Gate voltage: $V_g = -2$ volts
Saturation drift velocity: $v_s = 2 \times 10^5$ m/s

a. Calculate the pinch-off voltage.
b. Compute the velocity ratio.
c. Determine the saturation current at $V_g = 0$.
d. Find the drain current I_d.

Solution

a. From Eq. (6-2-3), the pinch-off voltage is

$$V_p = 1.6 \times 10^{-19} \times 8 \times 10^{23} \times 10^{-14}/(2 \times 8.854 \times 10^{-12} \times 13.1)$$
$$= 5.52 \text{ volts}$$

b. From Eq. (6-2-4), the velocity ratio is

$$\eta = 0.08 \times 5.52/(2 \times 10^5 \times 14 \times 10^{-6})$$
$$= 0.158$$

c. From Eq. (6-2-4), the saturation current at $V_g = 0$ is

$$I_p = \frac{qN_d\mu aZV_p}{2L}$$
$$= \frac{1.6 \times 10^{-19} \times 8 \times 10^{23} \times 0.08 \times 10^{-7} \times 36 \times 10^{-6} \times 5.52}{3 \times 14 \times 10^{-6}}$$
$$= 4.845 \text{ mA}$$

d. From Eq. (6-2-4), the u and ρ factors are

$$u = \left(\frac{5+2}{5.52}\right)^{1/2} = 1.126 \qquad u^2 = 1.268 \qquad u^3 = 1.428$$
$$\rho = \left(\frac{2}{5.52}\right)^{1/2} = 0.60 \qquad \rho^2 = 0.362 \qquad \rho^3 = 0.217$$

then the drain current is

$$I_d = 4.845 \times 10^{-3} \times \frac{3(1.268 - 0.362) - 2(1.428 - 0.217)}{1 - 0.158(1.268 - 0.362)}$$
$$= 4.845 \times 10^{-3} \times 0.259$$
$$= 1.26 \text{ mA}$$

6-2-5 Cutoff Frequency f_{co} and Maximum Oscillation Frequency f_{max}

The cutoff frequency of a Schottky barrier-gate FET in a circuit depends on the way in which the transistor is being made. In a wideband lumped circuit the cutoff frequency is expressed [7] as

$$f_{co} = \frac{g_m}{2\pi C_{gs}} = \frac{v_s}{4\pi L} \quad \text{Hz} \tag{6-2-11}$$

where g_m = transconductance

C_{gs} = gate-source capacitance $= \left.\dfrac{dQ}{dV_{gs}}\right|_{V_{gd}=\text{constant}}$

L = gate length

v_s = saturation drift velocity

It is interesting to note that the cutoff frequency of the lumped circuit analysis as shown in Eq. (6-2-11) is different from the charge-carrier transit-time cutoff frequency as shown in Eq. (5-1-58) by a factor of one-half.

The maximum frequency of oscillation depends on the device transconductance and the drain resistance in a distributed circuit. It is expressed [6] as

$$f_{\max} = \frac{f_{co}}{2}(g_m R_d)^{1/2} = \frac{f_{co}}{2}\left[\frac{\mu E_p(u_m - \rho)}{v_s(1 - u_m)}\right]^{1/2} \quad \text{Hz} \tag{6-2-12}$$

where R_d = drain resistance

g_m = device transconductance

E_p = electric field at the pinch-off region in the channel

u_m = saturation normalization of u

v_s, μ, and ρ are defined previously

For $\rho = 0$ (i.e. $V_{gs} = 0$) and $\eta \gg 1$, so that $f_{co} = \dfrac{v_s}{4\pi L}$ and $u_m = \left(\dfrac{3}{\eta}\right)^{1/3} \ll 1$.

We have

$$f_{\max} = \gamma \frac{v_s}{L}\left(\frac{3}{\eta}\right)^{1/6} \quad \text{Hz} \tag{6-2-13}$$

where $\gamma = 0.14$ for $\mu E_p/v_s = 13$ and $\gamma = 0.18$ for $\mu E_p/v_s = 20$ in the case of GaAs.

It has been found experimentally [6] that the maximum frequency of oscillation for a gallium arsenide FET with the gate length less than 10 μm is

$$f_{\max} = \frac{33 \times 10^3}{L} \quad \text{Hz} \tag{6-2-14}$$

where L = gate length in meters. The best value of L is 0.5 μm.

The maximum frequency of oscillation f_{max} is similar to the cutoff frequency f_{co} determined by the transit time. From Eq. (5-1-58) the charge-carrier transit-time cutoff frequency is

$$f_{co} = \frac{1}{2\pi\tau} = \frac{v_s}{2\pi L} \quad \text{Hz} \tag{6-2-15}$$

where $\tau = \dfrac{L}{v_s}$ is the transit time in seconds
L = gate length in meters
v_s = saturation drift velocity in meters per second

It is evident that the gallium arsenide FET has a better figure of merit than the silicon FET for an X-band amplifier because the saturation drift velocity $\mathcal{V}_s$ is 2×10^7 cm/sec for GaAs at an electric field of 3 kV/cm and 8×10^6 cm/sec for silicon at 15 kV/cm. In comparing Eq. (6-2-15) with Eq. (6-2-11), the difference is a factor of one-half.

The highest frequency of oscillation for maximum power gain with the input and output networks matched is given [8] as

$$f_{max} = \frac{f_{co}}{2}\left(\frac{R_d}{R_s + R_g + R_i}\right)^{1/2} \quad \text{Hz} \tag{6-2-16}$$

where R_d = drain resistance
R_s = source resistance
R_g = gate metallization resistance
R_i = input resistance

Example 6-2-3: Cutoff Frequency of a MESFET

A certain GaAs MESFET has the following parameters:

$R_g = 3\ \Omega$ $R_i = 2.5\ \Omega$ $g_m = 50\ \text{m}\mho$

$R_d = 450\ \Omega$ $R_s = 2.5\ \Omega$ $C_{gs} = 0.60\ \text{pF}$

a. Determine the cutoff frequency.

b. Find the maximum operating frequency.

Solution

a. From Eq. (6-2-11), the cutoff frequency is

$$f_{co} = \frac{g_m}{2\pi C_{gs}} = \frac{0.05}{2\pi \times 0.6 \times 10^{-12}}$$

$$= 13.26\ \text{GHz}$$

b. From Eq. (6-2-16), the maximum frequency is

$$f_{\max} = \frac{f_{co}}{2}\left(\frac{R_d}{R_s + R_g + R_i}\right)^{1/2}$$

$$= \frac{13.26 \times 10^9}{2}\left(\frac{450}{2.5 + 3 + 2.5}\right)^{1/2}$$

$$= 49.73 \text{ GHz}$$

6-3 HIGH ELECTRON-MOBILITY TRANSISTORS (HEMTs)

The evolution of high-speed GaAs integrated circuits (ICs) is the result of continuous technological progress utilizing the superior electronic properties of gallium arsenide compared with those of silicon. Electron mobility in the MESFET channel with typical donor concentrations of about 10^{17} cm^{-3} ranges from 4000 to 5000 cm^2/V·s at room temperature. The mobility in the channel at 77° K is not too much higher than at room temperature because of ionized impurity scattering. In undoped GaAs, however, electron mobility of 2 to 3 × 10^5 cm^2/V·s has been achieved at 77° K. The mobility of GaAs with feasibly high electron concentrations for facilitating the fabrication of devices was found to increase through modulation-doping techniques demonstrated in GaAs–AlGaAs superlattices [8]. A high electron-mobility transistor (HEMT), based on a modulation-doped GaAs–AlGaAs single heterojunction structure, was developed [9]. HEMTs have exhibited lower noise figure and higher gain at microwave frequencies up to 70 GHz, and it is possible to construct HEMT amplifiers at even higher frequencies of operation. The major improvements over MESFETs include shorter gate lengths, reduced gate and source contact resistances, and optimized doping profiles.

6-3-1 Physical Structure

The basic structure of a HEMT is a selectively doped GaAs–AlGaAs heterojunction structure as shown in Fig. 6-3-1.

An undoped GaAs layer and an Si-doped n-type AlGaAs layer are successively grown on a semi-insulating GaAs substrate. A two-dimensional electron gas (2-DEG) is created between the undoped and n-type layers. A buffer layer is sandwiched between the undoped GaAs layer and the semi-insulator substrate.

The HEMT can be fabricated by using the integrated-circuit techniques. Fig. 6-3-2 indicates the sequence for the self-aligned gate procedures in the fabrication of large-scale integration HEMTs, including the E-(enhacement-mode) and D-(depletion-mode) HEMTs.

The processing steps include the following:

1. Ohmic contact formation: The active region is isolated by a shallow mesa step (180 nm), which is almost achieved in a single process, and can be made nearly planar. The source and drain for E- and D-HEMTs are metallized with

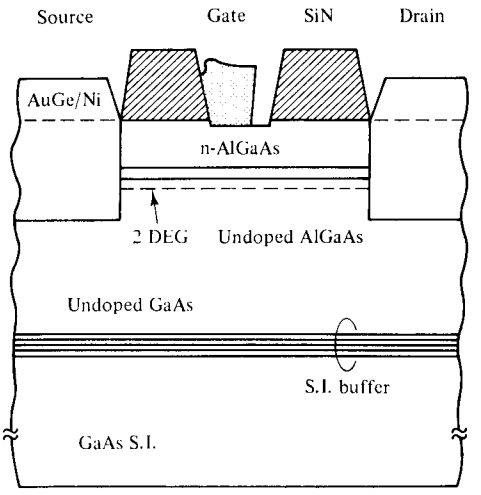


Figure 6-3-1 A cross section of a HEMT (*From K. Togashi et al. [10]; reprinted by permission of* Microwave Journal.)

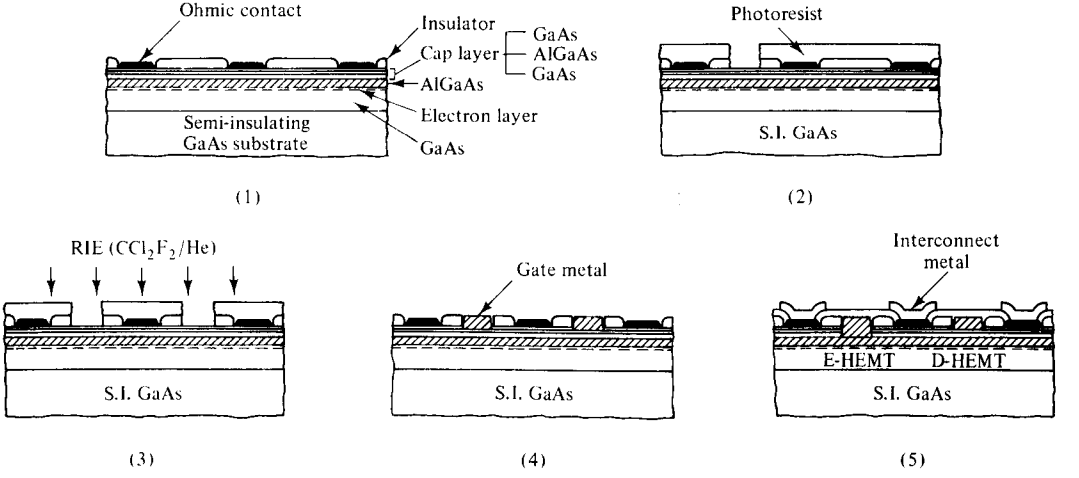


Figure 6-3-2 Processing steps for HEMT direct-coupled FET logic (DCFL) circuits. (*After M. Abe and others [9]; reprinted by permission of IEEE, Inc.*)

an AuGe eutectic alloy and an Au overlay alloy to produce ohmic contacts with the electron layer.

2. Opening gate windows: The fine gate patterns are formed for E-HEMTs as the top GaAs layer and thin $Al_{0.3}Ga_{0.7}As$ stopper are etched off by nonselective chemical etching.
3. Selective dry etching: With the same photoresist process for formation of gate patterns in D-HEMTs, selective dry etching is performed to remove the top GaAs layer for D-HEMTs and also to remove the GaAs layer under the thin $Al_{0.3}Ga_{0.7}As$ stopper for E-HEMTs.

4. Gate metallization: Schottky contacts for the E- and D-HEMT gate are provided by depositing Al. The Schottky gate contacts and the GaAs top layer for ohmic contacts are then self-aligned to achieve high-speed performance.
5. Interconnect metallization: Finally, electrical connections from the interconnecting metal, composed of Ti, Pt, and Au, to the device terminals are provided through contact holes etched in a crossover insulator film.

Figure 6-3-3 shows the cross-sectional view of a typical self-aligned structure of E- and D-HEMTs forming an inverter for the direct-coupled FET logic (DCFL) ciruit configuration [9].

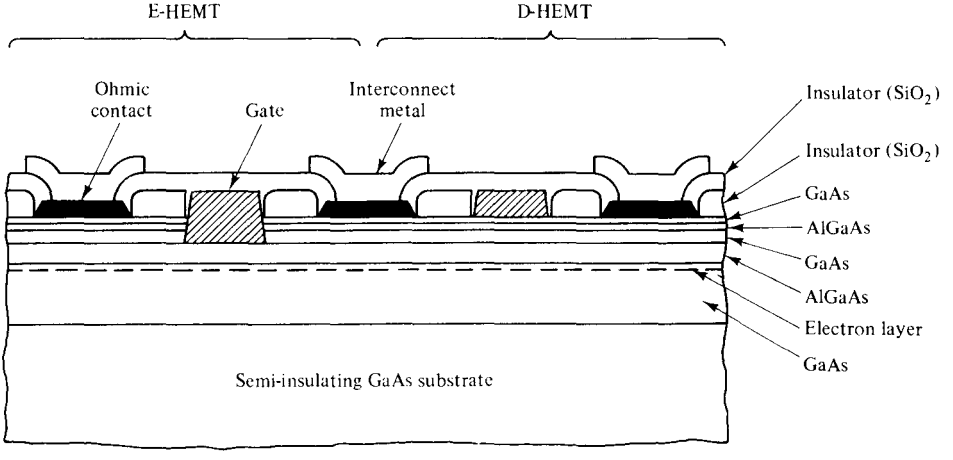


Figure 6-3-3 Cross-sectional view of a DCFL HEMT. (*After M. Abe et al. [9]; reprinted by permission of IEEE, Inc.*)

6-3-2 Operational Mechanism

Since GaAs has higher electron affinity, free electrons in the AlGaAs layer are transferred to the undoped GaAs layer where they form a two-dimensional high-mobility electron gas within 100 Å of the interface. The n-type AlGaAs layer of the HEMT is depleted completely through two depletion mechanisms (11):

1. Trapping of free electrons by surface states causes the surface depletion.
2. Transfer of electrons into the undoped GaAs layer brings about the interface depletion.

The Fermi energy level of the gate metal is matched to the pinning point, which is 1.2 eV below the conduction band. With the reduced AlGaAs layer thickness, the electrons supplied by donors in the AlGaAs layer are insufficient to pin the surface Fermi level, and the space-charge region is extended into the undoped GaAs layer. As a result, band bending is moving upward and the two-dimensional electron gas (2-DEG) does not appear. When a positive voltage higher than the threshold

voltage is applied to the gate, electrons accumulate at the interface and form a two-dimensional electron gas.

The electron concentration can control D-(depletion-mode) and E-(enhancement-mode) HEMT operations. As temperature decreases, electron mobility, which is about 8000 $cm^2/V \cdot s$ at 300° K, increases dramatically to 2×10^5 $cm^2/V \cdot s$ at 77° because of reduced phonon scattering. When the temperatures decrease further, the electron mobility of 1.5×10^6 $cm^2/V \cdot s$ at 50°K and 2.5×10^6 $cm^2/V \cdot s$ at 4.5°K have been demonstrated.

6-3-3 Performance Characteristics

High electron mobility transistor (HEMT) amplifiers for 40 to 70 GHz have been constructed. The 60-GHz amplifier exhibited a gain of 4.5 to 6.5 dB across the frequency band 56 to 62 GHz, and had an associated noise figure of 6 dB measured at 57.5 GHz. The 72-GHz amplifier achieved a gain of 4 to 5 dB with a bandwidth of 2.5 GHz [11].

Current–voltage (*I–V*) characteristics. The drain current can be evaluated from the following basic equation

$$I_{ds} = qn(z)Wv(z) \tag{6-3-1}$$

where q = electron charge
$n(z)$ = concentration of the two-dimensional electron gas
W = gate width
$v(z)$ = electron velocity

Figure 6-3-4 shows the *I-V* characteristics of a HEMT amplifier with $W = 150\ \mu m$ and L_g (gate length) $= 0.6\ \mu m$ at 30 GHz.

The major advantages of a HEMT are higher frequency, lower noise, and higher speed. Table 6-3-1 compares HEMT data with other semiconductor electronic devices.

Example 6-3-1: Current of a HEMT

A HEMT has the following parameters:

Gate width:	$W = 150\ \mu m$
Electron velocity:	$v(z) = 2 \times 10^5$ m/s
Two-dimensional electron-gas density:	$n(z) = 5.21 \times 10^{15}\ m^{-2}$

Determine the drain current of the HEMT.

Solution From Eq. (6-3-1), the drain current is

$$\begin{aligned} I_{ds} &= qn(z)Wv(z) \\ &= 1.6 \times 10^{-19} \times 5.21 \times 10^{15} \times 150 \times 10^{-6} \times 2 \times 10^5 \\ &= 25\ \text{mA} \end{aligned}$$

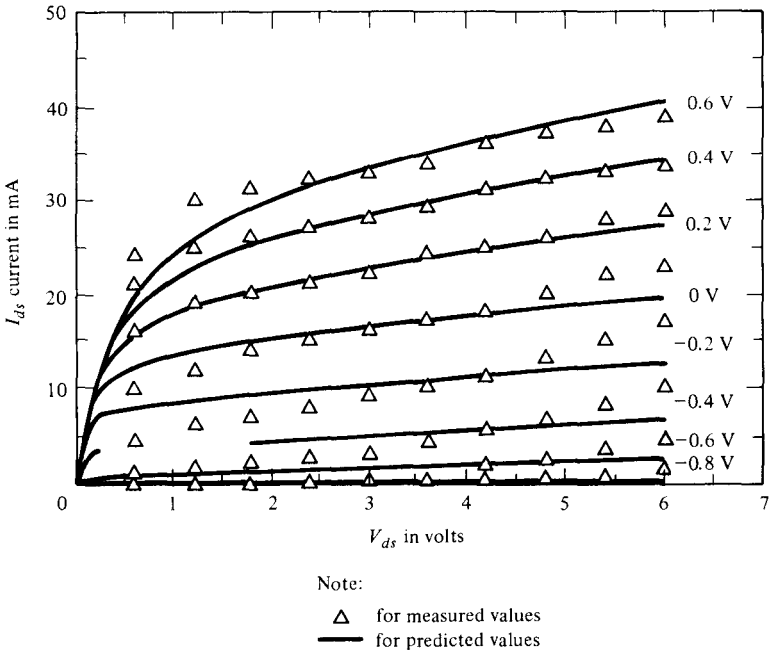


Figure 6-3-4 *I-V* characteristics of a HEMT.

TABLE 6-3-1 HEMT PERFORMANCE COMPARED WITH OTHER DEVICES

Device	Frequency (GHz)	Noise	Power	Speed
HEMT	Up to 70	Very Good	Very Good	Excellent
GaAs MESFET	40	Good	Good	Good
GaAs–AlGaAs HBT*	20	Good	Good	Excellent
Si MOSFET	10	Poor	Very good	Very poor
Si bipolar transistor	1	Poor	Poor	Good

* HBT = heterojunction bipolar transistor

Equivalent circuit. In order to predict or calculate the values for a small- or large-signal HEMT amplifier, the following high-frequency equivalent circuit, shown in Fig. 6-3-5, may be useful.

It is difficult to compare the optimized performance of most major semiconductor devices. The switching delay time of GaAs MESFETs is two or three times longer than that of HEMTs. The GaAs–AlGaAs heterojunction bipolar transistor (HBT) can achieve the same high-speed performance as the HEMT. The ultimate speed capability, limited by cutoff frequency f_T, is more than 100 GHz, and the HBT also has the merit of flexible fan-out loading capability. The silicon MOSFET and the bipolar transistor have excellent performance in threshold voltage uniformity and controllability with no material problems, and they are easy to fabricate despite complex processing steps. HEMTs are very promising devices for high-speed, very large-scale integration (VLSI) with low-power dissipation, but they require new

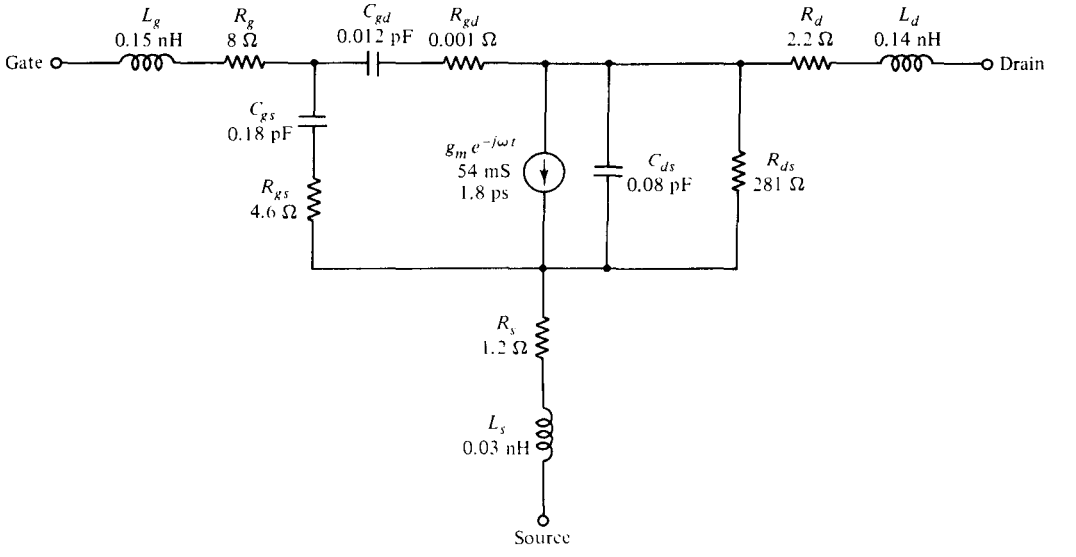


Figure 6-3-5 Equivalent circuit of a HEMT.

technological breakthroughs to achieve the large-scale integration (LSI) quality of GaAs–AlGaAs material. Such technologies include molecular-beam epitaxy (MBE), organic metal-vapor phase epitaxy (OMPVE), and self-alignment device fabrications. The excellent controllability of MBE growth can regulate the ratio of standard deviation of threshold voltage to the logic voltage swing.

The vertical threshold sensitivity is defined by the differential threshold voltage to the thickness of the $Al_xGa_{1-x}As$ layer and is expressed as

$$\frac{dV_{th}}{d\ell} = -[2qN_d(\psi_{ms} - \Delta E_c - V_{th})/\epsilon]^{1/2} \tag{6-3-2}$$

where V_{th} = threshold voltage in volts
ℓ = AlGaAs layer thickness in meters
q = electron charge
N_d = donor concentration
ψ_{ms} = metal-semicondcutor Schottky barrier potential between Al and GaAs
E_c = conduction bandedge difference between GaAs and AlGaAs
$\epsilon = \epsilon_o\epsilon_r$ is the permittivity of AlGaAs
ϵ_r = dielectric constant of AlGaAs

Example 6-3-2: Sensitivity of HEMT

A HEMT has the following parameters:

Threshold voltage:	$V_{th} = 0.13$ V
Donor concentration:	$N_d = 2 \times 10^{24}$ m^{-3}
Metal-semiconductor Schottky barrier potential:	$\psi_{ms} = 0.8$ V

GaAs bandgap:	$E_{gg} = 1.43$ V
AlGaAs bandgap:	$E_{ga} = 1.80$ V
AlGaAs dielectric constant	$\epsilon_r = 4.43$

Compute:

a. The conduction band-edge difference between GaAs and AlGaAs

b. The sensitivity of the HEMT

Solution

a. The conduction band-edge difference is

$$\Delta E_c = E_{ga} - E_{gg} = 1.80 - 1.43 = 0.37 \text{ V}$$

b. The sensitivity of the HEMT is

$$\frac{dV_{th}}{d\ell} = -[2qN_d(\psi_{ms} - \Delta E_c - V_{th})/\epsilon]^{1/2}$$

$$= -[2 \times 1.6 \times 10^{-19} \times 2 \times 10^{24}(0.80 - 0.37 - 0.13)/(8.854 \times 10^{-12} \times 4.43)]^{1/2}$$

$$= -\left[\frac{0.49 \times 10^4}{10^{-12}}\right]^{1/2} = -70 \text{ mV/nm}$$

$$\left|\frac{dV_{th}}{d}\right| = 70 \text{ mV/nm}$$

6-3-4 Electronic Applications

The switching speed of a HEMT is about three times as fast as that of a GaAs MESFET. The largest-scale logic integrated circuit (IC) with HEMT technology has achieved the highest speed ever reported among 8 × 8 bit multipliers. The switching delay time of a HEMT is below 10 picosecond with a power dissipation reported at about 100 μW. Therefore, HEMTs are promising devices for very large-scale integration, especially in very high-speed supercomputers, star wars, and space communications.

Information processing in the 1990s will require ultrahigh-speed computers, having high-speed large-scale integration circuits with logic delays in the sub-hundred-picosecond range. A 4K × 1 bit static random-access memory (SRAM) device consists of a memory cell of 55 μm × 39 μm. Its normal read-write operation was confirmed both at 300° K and 77° K. The minimum address access time obtained was 2.0 nanosecond with a chip dissipation power of 1.6 W and a supply voltage of 1.54 V. The HEMT SRAMs have demonstrated better performance than the SiMOS, BJT, and GaAs MESFET SRAMs.

6-4 METAL-OXIDE-SEMICONDUCTOR FIELD-EFFECT TRANSISTORS (MOSFETs)

The metal-oxide-semiconductor field-effect transistor (MOSFET) is a four-terminal device, and its current flow is controlled by an applied vertical electric field. The four terminals are denoted as the *source, gate, drain,* and *substrate*. When the gate bias voltage is zero, the two back-to-back p-n junctions between the source and drain prevent current flow in either direction. When a positive voltage is applied to the gate with respect to the source (source and substrate are common), negative charges are induced in the channel to provide current flow. Since the current is controlled by the electric field, this type of device is called the *junction field-effect transistor* (JFET). The MOSFETs have superseded the bipolar junction transistors in many electronic applications because their structures are simple and their costs are low. In addition, the n-channel MOSFET (NMOS), p-channel MOSFET (PMOS), complementary MOSFET (CMOS), logic-gate memories, and the charge-coupled devices (CCDs) have emerged as important semiconductor electronic devices. All these devices are discussed in this section.

The metal-insulator-semiconductor field-effect transistor (MISFET) may be formed by a metal such as aluminum (Al) and a semiconductor, such as Ge, Si, or GaAs, with an insulator such as SiO_2, Si_3N_4, or Al_2O_3 sandwiched between. If the structure is in the form of Al-SiO_2-Si, it is called a MOSFET. This device is very useful in very large-scale integrated microwave circuits. In the near future, a microwave-device chip of 1-μm dimension containing 1 million or more devices will be commercially available. The basic component of a MOSFET is the MIS diode which was described previously.

6-4-1 Physical Structures

The metal-oxide-semiconductor field-effect transistor (MOSFET) is a four-terminal device. There are both n-channel and p-channel MOSFETs. The n-channel MOSFET consists of a slightly doped p-type semiconductor substrate into which two highly doped n^+ sections are diffused, as shown in Fig. 6-4-1. These n^+ sections, which act as the source and the drain, are separated by about 0.5 μm. A thin layer of insulating silicon dioxide (SiO_2) is grown over the surface of the structure. The metal contact on the insulator is called the *gate*.

Similarly, the p-channel MOSFET is made of a slightly doped n-type semiconductor with two highly doped p^+-type regions for the source and drain. The heavily doped polysilicon or a combination of silicide and polysilicon can also be used as the gate electrode. In practice, a MOSFET is commonly surrounded by a thick oxide to isolate it from the adjacent devices in a microwave integrated circuit. The basic device parameters of a MOSFET are as follows: L is the channel length, which is the distance between the two n^+-p junctions just beneath the insulator (say, 0.5 μm), Z is the channel depth (say, 5μm), d is the insulator thickness (say, 0.1 μm), and r_j is the junction thickness of the n^+ section (say, 0.2 μm).

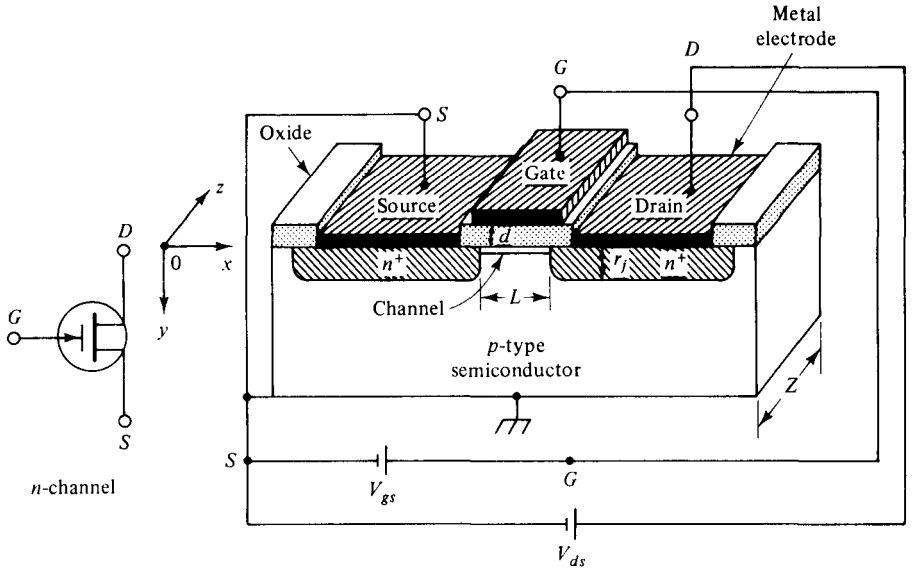


Figure 6-4-1 Schematic diagram of an n-channel MOSFET.

6-4-2 Electronic Mechanism

When no voltage is applied to the gate of an n-channel MOSFET, the connection between the source electrode and the drain electrode corresponds to a link of two p-n junctions connected back-to-back. The only current that can flow from the source to the drain is the reverse leakage current. When a positive voltage is applied to the gate relative to the source (the semiconductor substrate is grounded or connected to the source), positive charges are deposited on the gate metal. As a result, negative charges are induced in the p-type semiconductor at the insulator-semiconductor interface. A depletion layer with a thin surface region containing mobile electrons is formed. These induced electrons form the n-channel of the MOSFET and allow the current to flow from the drain electrode to the source electrode. For a given value of the gate voltage V_g, the drain current I_d will be saturated for some drain voltages V_d.

A minimum gate voltage is required to induce the channel, and it is called the *threshold voltage* V_{th}. For an n-channel MOSFET, the positive gate voltage V_g must be larger than the threshold voltage V_{th} before a conducting n-channel (mobile electrons) is induced. Similarly, for a p-channel MOSFET, the gate voltage V_g must be more negative than the threshold voltage V_{th} before the p-channel (mobile holes) is formed.

6-4-3 Modes of Operation

There are basically four modes of operation for n-channel and p-channel MOSFETs.

1. n-Channel Enhancement Mode (normally OFF). When the gate voltage is zero, the channel conductance is very low and it is not conducting. A positive

voltage must be applied to the gate to form an n channel for conduction. The drain current is enhanced by the positive voltage. This type is called the enhancement-mode (normally OFF) n-channel MOSFET.

2. n-Channel Depletion Mode (normally ON). If an n channel exists at equilibrium (that is, at zero bias), a negative gate voltage must be applied to deplete the carriers in the channel. In effect, the channel conductance is reduced, and the device is turned OFF. This type is called the depletion-mode (normally ON) n-channel MOSFET.
3. p-Channel Enhancement Mode (normally OFF). A negative voltage must be applied to the gate to induce a p channel for conduction. This type is called the enhancement-mode (normally OFF) p-channel MOSFET.
4. p-Channel Depletion Mode (normally ON). A positive voltage must be applied to the gate to deplete the carriers in the channel for nonconduction. This type is called the depletion-mode (normally ON) p-channel MOSFET.

Figure 6-4-2 shows the four modes of the MOSFETs, and Fig. 6-4-3 illustrates their electric symbols, output I-V characteristics, and transfer characteristics.

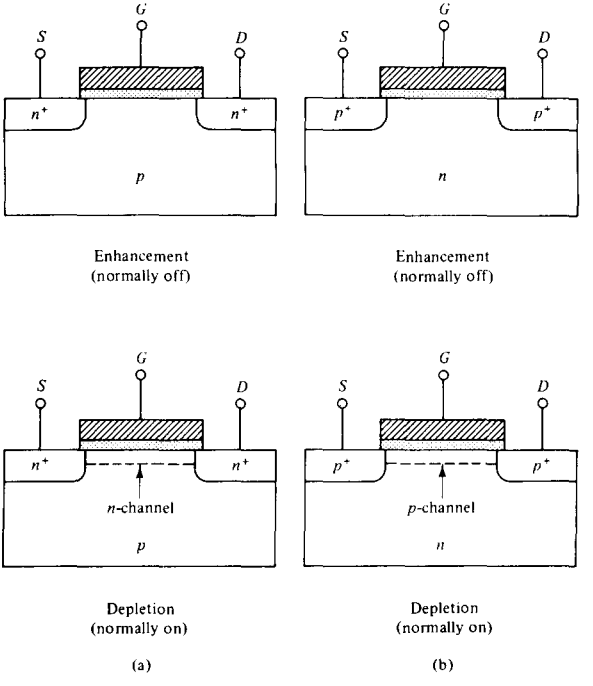


Figure 6-4-2 Four modes of operation for MOSFETs: (a) n channel and (b) p channel.

6-4-4 Drain Current and Transconductance

Drain current. The drain current I_d of the MOSFET is dependent of the drain voltage V_d. It first increases linearly with the drain voltage in the linear region and then gradually levels off to a saturated value in the saturation region. Figure 6-4-4 shows the current-voltage characteristic curves of an n-channel MOSFET [12].

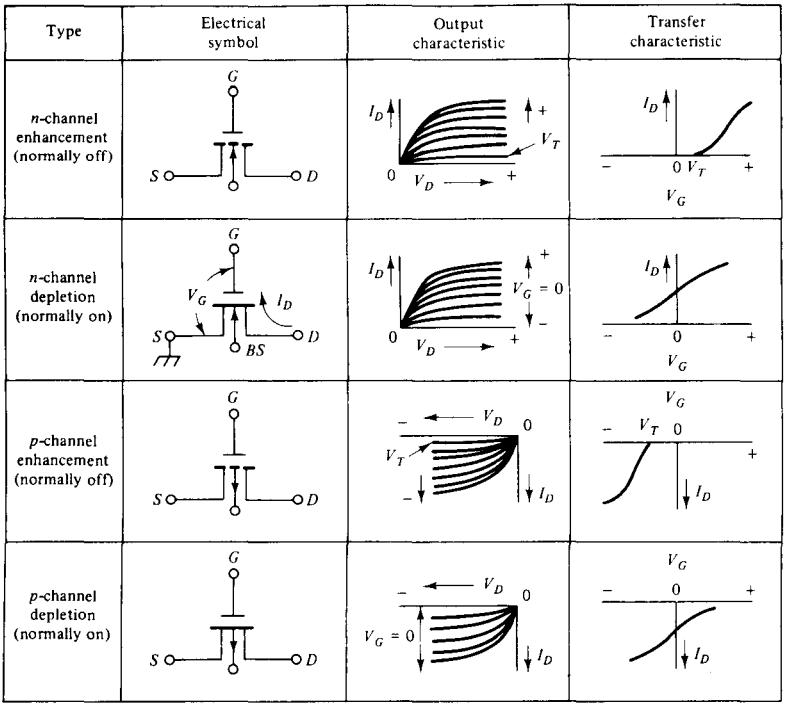


Figure 6-4-3 Electric symbols and output and transfer characteristics of the four modes of MOSFETs.

The drain current I_d is given by [12] as

$$I_d = \frac{Z}{L}\mu_n C_i\left\{\left(V_g - 2\psi_b - \frac{V_d}{2}\right)V_d - \frac{2}{3C_i}(2\epsilon_s q N_a)^{1/2}[(V_d + 2\psi_b)^{1/2} - (2\psi_b)^{1/2}]\right\} \tag{6-4-1}$$

where μ_n = electron carrier mobility

$C_i = \dfrac{\epsilon_i}{d}$ is the insulator capacitance per unit area

ϵ_i = insulator permittivity

V_g = gate voltage

$\psi_b = (E_i - E_F)/q$ is the potential difference between the Fermi level E_F and the intrinsic Fermi level E_i

V_d = drain voltage

ϵ_s = semiconductor permittivity

q = carrier charge

N_a = acceptor concentration

In the linear region, the drain voltage is small and Eq. (6-4-1) becomes

$$I_d \simeq \frac{Z}{L}\mu_n C_i\left[(V_g - V_{th})V_d - \left(\frac{1}{2} + \frac{\sqrt{\epsilon_s q N_a/\psi_b}}{4C_i}\right)V_d^2\right] \tag{6-4-2}$$

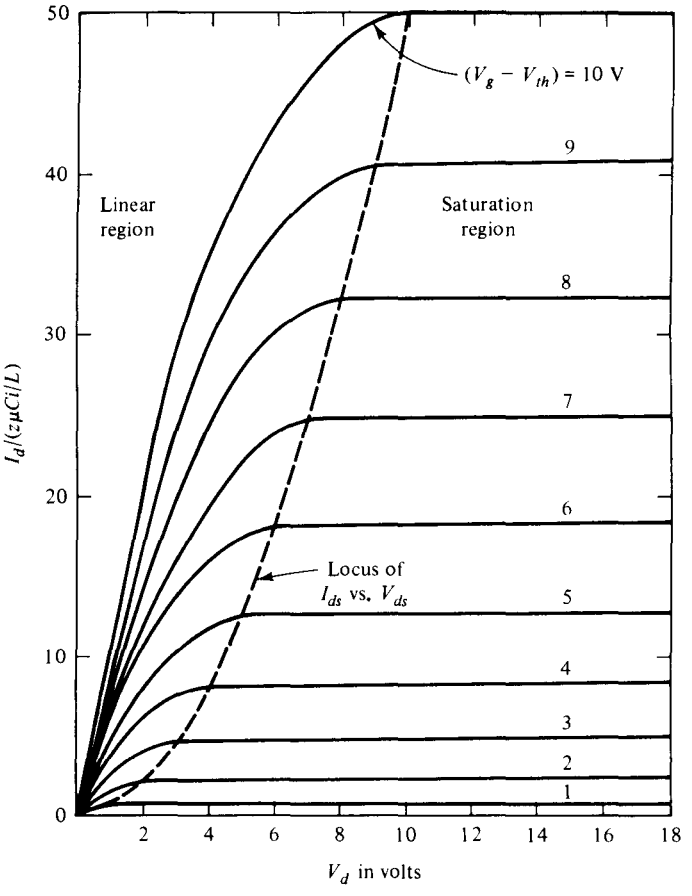


Figure 6-4-4 Current-Voltage (I-V) curves of an n-channel MOSFET.

or

$$I_d \simeq \frac{Z}{L}\mu_n C_i(V_g - V_{th})V_d \qquad \text{for } V_d \ll (V_g - V_{th}) \tag{6-4-3}$$

where $V_{th} = 2\psi_b + \frac{2}{C_i}(\epsilon_s q N_a \psi_b)^{1/2}$

In the saturation region, the drain current is given by

$$I_{d\,\text{sat}} \simeq \frac{mZ}{L}\mu_n C_i(V_g - V_{th})^2 \tag{6-4-4}$$

where $m = 0.5$ is the low doping factor, and $V_{d\,\text{sat}} \simeq V_g - V_{th}$ may be assumed

Transconductance. The transconductance g_m, which is also called the mutual conductance, in the linear region can be found from Eq. (6-4-3) as

$$g_m = \frac{\partial I_d}{\partial V_g}\bigg|_{V_d=\text{constant}} = \frac{Z}{L}\mu_n C_i V_d \tag{6-4-5}$$

In the saturation region, the transconductance becomes

$$g_{m\,\text{sat}} = \frac{2mZ}{L}\mu_n C_i(V_g - V_{th}) \tag{6-4-6}$$

The channel conductance g_d is given by

$$g_d = \frac{\partial I_d}{\partial V_d}\bigg|_{V_g=\text{constant}} = \frac{Z}{L}\mu_n C_i(V_g - V_{th}) \tag{6-4-7}$$

All equations derived here so far are based on the idealized n-channel MOSFET. For an idealized p-channel MOSFET, all voltages V_g, V_d, and V_{th} are negative, and the drain current I_d flows from the source to the drain. For a real n-channel MOSFET (say, Al-Oxide-Si structure), the saturation drain current is

$$I_{d\,\text{sat}} = ZC_i(V_g - V_{th})v_s \tag{6-4-8}$$

and the transconductance becomes

$$g_m = ZC_i v_s \tag{6-4-9}$$

where $v_s = L/\tau$ is the carrier drift velocity

The threshold voltage V_{th} is given by

$$V_{th} = \frac{\phi_{ms}}{q} - \frac{Q_f}{C_i} + 2\psi_b + \frac{2}{C_i}(\epsilon_s q N_a \psi_b)^{1/2} \tag{6-4-10}$$

where $\phi_{ms} = \phi_m - \phi_s$ is the work function difference (in eV) between the metal work function ϕ_m and the semiconductor work function ϕ_s

Q_f = fixed oxide charges

Example 6-4-1: Threshold Voltage of an Ideal MOSFET

A certain p-channel MOSFET has the following parameters:

Doping concentration:	$N_a = 3 \times 10^{17}\ \text{cm}^{-3}$
Relative dielectric constant:	$\epsilon_r = 11.8$
Relative dielectric constant of SiO_2:	$\epsilon_{ir} = 4$
Insulator depth:	$d = 0.01\ \mu\text{m}$
Operating temperature:	$T = 300°\text{K}$

a. Calculate the surface potential ψ_s (inv) for strong inversion.

b. Compute the insulator capacitance.

c. Determine the threshold voltage.

Solution

a. From Eq. (6-4-4), the surface potential for strong inversion is

$$\psi_{s\,\text{inv}} = 2 \times 26 \times 10^{-3}\, \ell n\left(\frac{3 \times 10^{17}}{1.5 \times 10^{10}}\right)$$

$$= 0.874 \text{ volt}$$

b. From Eq. (6-4-1), the insulator capacitance is

$$C_i = \frac{\epsilon_i}{d} = \frac{4 \times 8.854 \times 10^{-12}}{0.01 \times 10^{-6}} = 3.54 \text{ mF/m}^2$$

c. From Eq. (6-4-3), the threshold voltage is

$$V_{th} = 0.874 + \frac{2}{3.54 \times 10^{-3}} \times (8.854 \times 10^{-12} \times 11.8 \times 1.6 \times 10^{-19} \times 3 \times 10^{23} \times 0.437)^{1/2}$$

$$= 0.874 + 0.56 \times 10^{3} \times 14.80 \times 10^{-4}$$

$$= 1.70 \text{ volts}$$

6-4-5 Maximum Operating Frequency

The maximum operating frequency of a MOSFET is determined by its circuit parameters. A common-source equivalent circuit of a MOSFET is shown in Fig. 6-4-5.

where g_{in} = input conductance due to the leakage current. Since the leakage current is very small, say 10^{-10} A/cm^2, g_{in} is negligible
$C_{\text{in}} = ZLC_i$ is the input capacitance
C_{fb} = feedback capacitance
$g_{\text{out}} = g_d$ is output conductance
$C_{\text{out}} = C_i C_s/(C_i + C_s)$ is the sum of the two p-n junction capacitances in series with the semiconductor capacitance per unit area

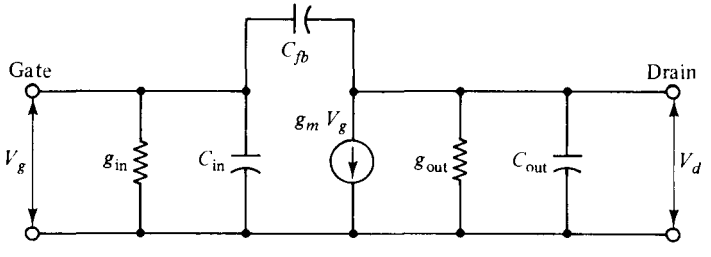


Figure 6-4-5 Equivalent circuit of a common-source MOSFET.

The maximum operating frequency of a MOSFET in the linear region can be expressed as

$$f_m = \frac{\omega_m}{2\pi} = \frac{g_m}{2\pi C_{\text{in}}} = \frac{\mu_n V_d}{2\pi L^2} \tag{6-4-11}$$

In the saturation region, $V_g \gg V_{th}$, the transconductance is reduced to

$$g_{m\,\text{sat}} = \frac{Z}{L}\mu_n C_i V_g = ZC_i v_s \tag{6-4-12}$$

6-4-6 Electronic Applications

The MOSFETs are often used as power amplifiers because they offer two advantages over MESFETs and JFETs.

1. In the active region of an enhancement-mode MOSFET, the input capacitance and the transconductance are almost independent of gate voltage, and the output capacitance is independent of the drain voltage. This leads to very linear (Class A) power amplification.
2. The active gate-voltage range can be larger because n-channel depletion-type MOSFETs can be operated from the depletion-mode region $(-V_g)$ to the enhancement-mode region $(+V_g)$.

Example 6-4-2: Characteristics of a MOSFET

A certain n-channel MOSFET has the following parameters:

Channel length:	$L = 4\ \mu\text{m}$
Channel depth:	$Z = 12\ \mu\text{m}$
Insulator thickness:	$d = 0.05\ \mu\text{m}$
Gate voltage:	$V_g = 5\ \text{V}$
Doping factor:	$m = 1$
Threshold voltage:	$V_{th} = 0.10\ \text{V}$
Electron mobility:	$\mu_n = 1350 \times 10^{-4}\ \text{m}^2/\text{V}\cdot\text{s}$
Electron velocity:	$v_s = 1.70 \times 10^7\ \text{cm/s}$
Relative dielectric constant of SiO_2:	$\epsilon_{ir} = 3.9$

a. Compute the insulator capacitance in F/m^2.
b. Calculate the saturation drain current in mA.
c. Determine the transconductance in the saturation region in millimhos.
d. Estimate the maximum operating frequency in the saturation region in GHz.

Solution

a. The capacitance of the insulator SiO_2 is

$$C_i = \frac{\epsilon_i}{d} = \frac{3.9 \times 8.854 \times 1C^{-12}}{0.05 \times 10^{-6}} = 6.91 \times 10^{-4}\,\text{F/m}^2$$

b. From Eq. (6-4-8), the saturation drain current is

$$\begin{aligned} I_{d\,\text{sat}} &= ZC_i(V_g - V_{th})v_s \\ &= 12 \times 10^{-6} \times 6.91 \times 10^{-4} \times (5 - 0.1) \times 1.7 \times 10^5 \\ &= 6.91\ \text{mA} \end{aligned}$$

c. From Eq. (6-4-9), the transconductance in the saturation region is

$$\begin{aligned} g_{m\,\text{sat}} &= ZC_i v_s \\ &= 12 \times 10^{-6} \times 6.91 \times 10^{-4} \times 1.7 \times 10^5 \\ &= 1.41\ \text{m}\mho \end{aligned}$$

d. From Eq. (6-4-13), the maximum operating frequency is

$$f_m = \frac{v_s}{2\pi L} = \frac{1.7 \times 10^5}{2\pi \times 4 \times 10^{-6}} = 6.76\ \text{GHz}$$

6-5 MOS TRANSISTORS AND MEMORY DEVICES

As discussed in Section 6-2, the source, channel, and the drain of the MOS transistor are surrounded by a depletion region, so there is no need to isolate individual components. This elimination of isolation regions in MOS transistors allows a much greater packing density on a semiconductor chip than is possible with bipolar junction transistors. The MOSFET can be subdivided into two groups:

1. The n-channel MOSFET is commonly referred to as an *NMOS*.
2. The complementary MOSFET is usually called a *CMOS*. The CMOS provides n-channel and p-channel MOSFETs on the same chip.

The fabrication technology for an NMOS is much simpler than for the bipolar transistor. The CMOS circuit has lower power dissipation than both the bipolar transistor and the NMOS circuits. So both NMOS and CMOS devices are very useful in high density integrated circuits.

6-5-1 NMOS Devices

The metal-oxide-semiconductor field-effect transistor (MOSFET) is the dominant device used in very large-scale integration (VLSI) circuits. In the 1960s, the *p-channel MOS* (*PMOS*) was originally used in integrated circuits. *n-channel MOS* (*NMOS*)

devices, however, have dominated the IC market since the 1970s because their electron mobility is higher than that of holes.

NMOS structure. Figure 6-5-1 shows a three-dimensional view of an NMOS logic circuit.

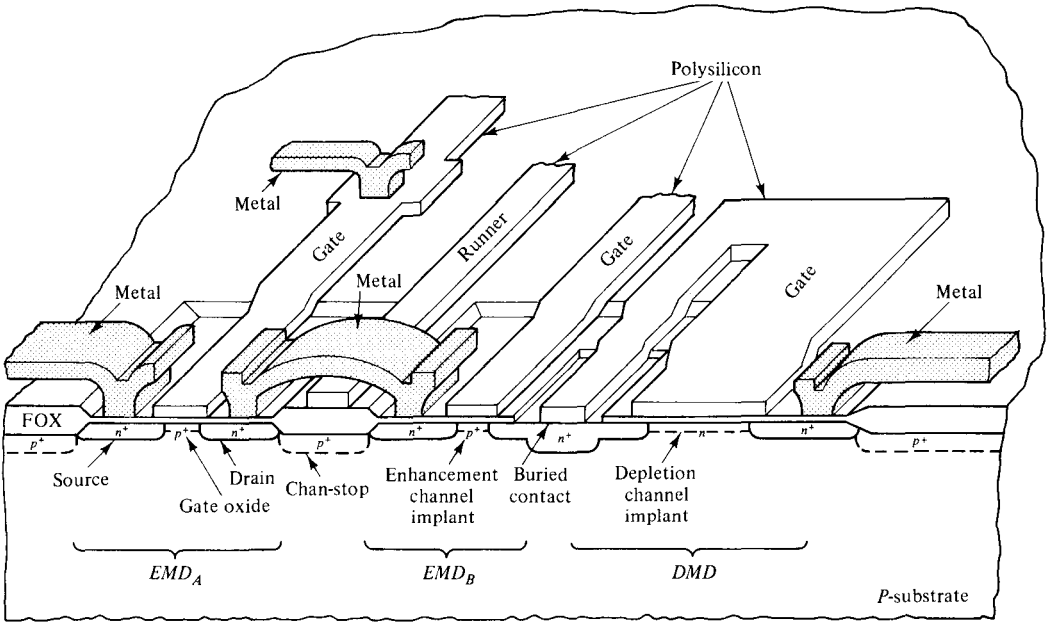
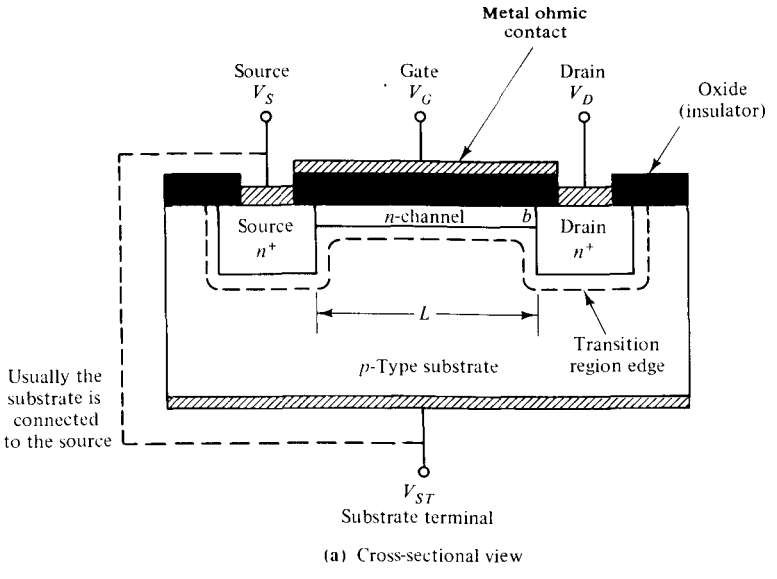


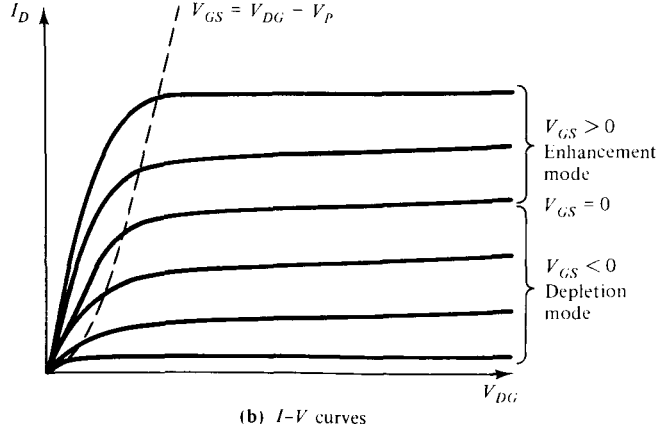
Figure 6-5-1 Three-dimensional view of an NMOS logic circuit. (*After Parrillo [13]; reprinted by permission of the Bell Laboratory.*)

From Fig. 6-5-1, it can be seen that two enhancement-mode (normally OFF) devices (EMD_A and EMD_B) are in series with a depletion-mode (normally ON) device (DMD). A field oxide (FOX) surrounds the transistors, and the gate and source of the DMD are connected at the buried contact. An intermediate dielectric layer separates the overlying metal layer from the underlying layers. In the JFET the high input resistance is obtained from the reverse-biased p-n junction. In the MOSFET the extremely high input resistance ($\sim 10^{14}$ ohms) is made possible by the insulator.

There are two basic structures for MOSFETs: the depletion type and the induced type as shown in Figs. 6-5-2 and 6-5-3, respectively. The major difference between them is that with the terminals of the device open-circuited, the depletion type has a conducting channel that links the drain to the source; the induced type has a channel of opposite type to that of the drain and the source linking the two regions. When the device has p-type source and drain regions, it is called the p-channel MOSFET or PMOS.

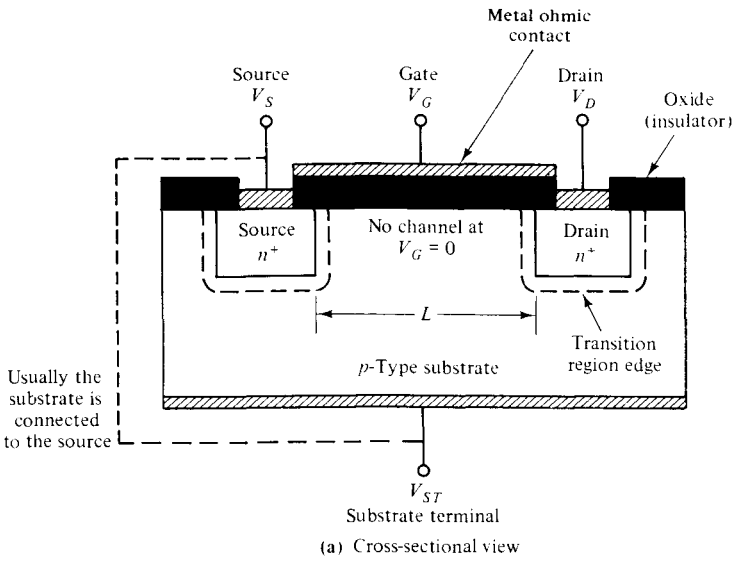


(a) Cross-sectional view

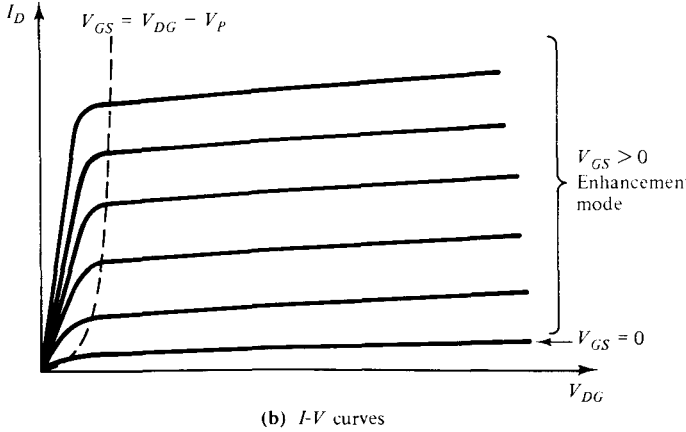


(b) I–V curves

Figure 6-5-2 n-channel depletion-type MOSFET.



(a) Cross-sectional view



(b) I-V curves

Figure 6-5-3 n-channel induced-type MOSFET.

The structures of enhancement and depletion modes refer to the relative increase or decrease of the majority carrier density in the channel connecting the source to the drain. If a given gate bias tends to increase the majority carrier density in the channel, the device is said to be operated in the enhancement mode (normally OFF). Hence, if the gate in an NMOS is biased by a positive voltage with respect to the substrate, which tends to drain more electrons into the n-type channel, it is said to be operated in the enhancement mode. If a negative gate potential with respect to the substrate is applied in order to diminish the electron density in the n channel, then it is said to be operated in the depletion mode. For a p-channel MOSFET (PMOS), when the negative gate potential with respect to the substrate is biased, the device is operated in the enhancement mode; and when the positive gate voltage is applied, the device is operated in the depletion mode. When a MOS is operated in the enhancement mode, the drain current is higher because the majority carrier density is higher. When, however, the MOS is operated in the depletion mode, the drain current is lower because the majority carrier density is lower.

NMOS operation. The operation of an NMOS can be described as a logic gate as shown in Fig. 6-5-4.

Two enhancement-mode devices (EMD) are in series with a depletion-mode device (DMD), and the three transistors are connected between the positive power supply V_{DD} and ground V_{SS} reference. The DMD is normally on at $V_{GS} = 0$ and acts as a current source for the two EMDs. Gates A and B of the two EMDs serve as inputs to the logic circuit, and the DMD's gate-source connection is the output electrode of the logic circuit. The output voltage of the two-input NAND circuit is low only when both EMDs are turned on at their logic-high level.

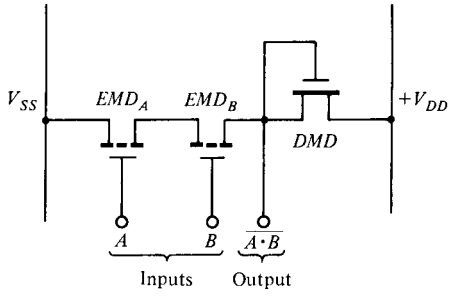
NMOS devices can be also used as NOR-gate circuits, as shown in Fig. 6-5-5.

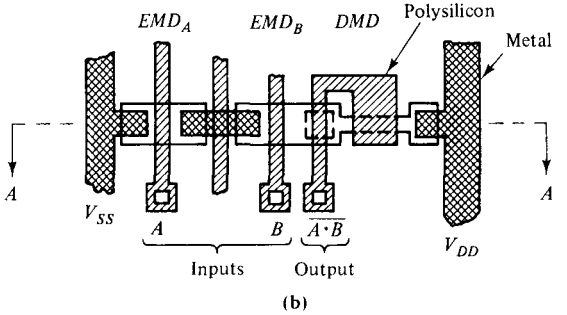
The two-input enhancement-mode NMOS devices are called *drivers,* and the depletion-mode MOSFET, *the load.* When there is a logic *O*-state input signal (low voltage at V_{i1}) at the driver device, the device has a very small channel current and the output is at *1* state (the output voltage is close to V_{DD}). But when the input signal is at *1* state, the device conducts a large current with a small voltage drop across the driver, and the output is at *O* state. The input and output are inverted and a NOR logic is achieved.

6-5-2 CMOS Devices

The *complementary MOS* (*CMOS*) is made of both NMOS and PMOS devices, and its power consumption is quite low. In some CMOS designs, the NMOS circuit is incorporated in domino-CMOS to take advantage of the NMOS's high speed and the CMOS's low power.

CMOS structure. There are three structures of CMOS devices: n tub, p tub, and twin tub. When a tub is formed in a p-type substrate, the device is called an n *tub,* just as when in an n-type substrate it is called a p *tub.* If an n-tub and a p-tub are combined on the same substrate, the device is referred to as a *twin tub.* A tub is





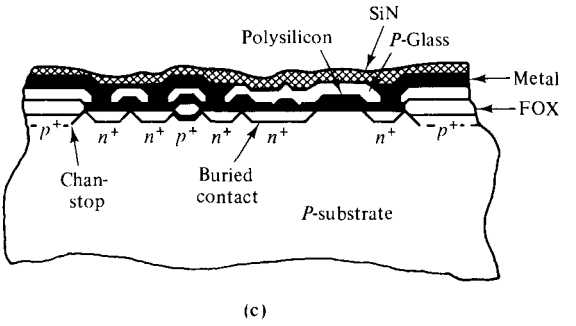


Figure 6-5-4 Two-input NAND logic gate. (*After Parrillo [13]; reprinted by permission of the Bell Laboratory.*)

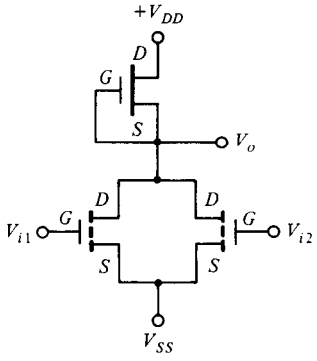
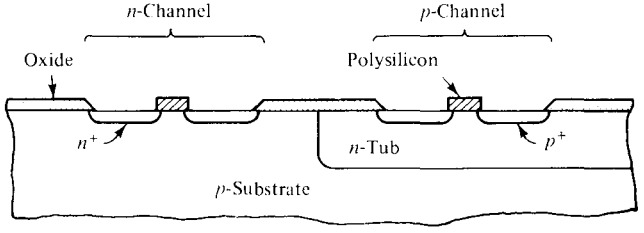
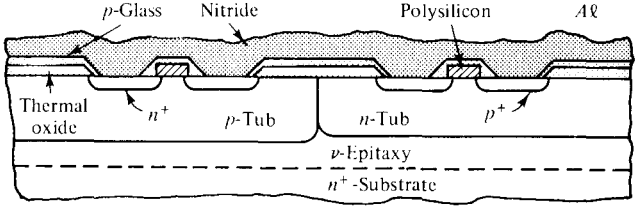


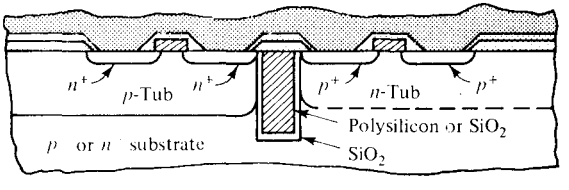
Figure 6-5-5 NOR logic gate.



(a) n tub



(b) p tub



(c) Twin tub

Figure 6-5-6 CMOS structures. (*After L.C. Parrillo [13]; reprinted by permission of the Bell Laboratory.*)

also called a well, and it can be produced by extra diffusion steps. Figure 6-5-6 shows the structures of an n tub, a p tub, and a twin tub.

CMOS operation. The operation of a CMOS inverter is shown in Fig. 6-5-7. The p-channel transistor is formed in the n-type structure, and the n-channel transistor is grown in the p region, which in turn is formed in the n-type substrate. The p region acts as the n-channel transistor's substrate (back gate) and it is commonly referred to as a tub or well. The gates of the n- and p-channel transistors are connected and serve as the input to the inverter. The common drains of each device are the output of the inverter. The threshold voltage of the n- and p-channel transistors are V_{tn} and V_{tp}, respectively, ($V_{tp} < 0$). Figure 6-5-7(c) shows the dependence of the output voltage V_o on the input voltage V_I of the CMOS inverter. For $V_I = 0$, the n-channel transistor is OFF ($V_I \ll V_{tn}$), while the p-channel transistor is heavily turned ON (that is, the gate-to-source voltage of the p channel is $-V_{DD}$, which is much more negative than V_{tp}). Therefore, the output voltage is $V_o = V_{DD}$. As the input voltage V_I is increased above zero, the n-channel transistor eventually is turned

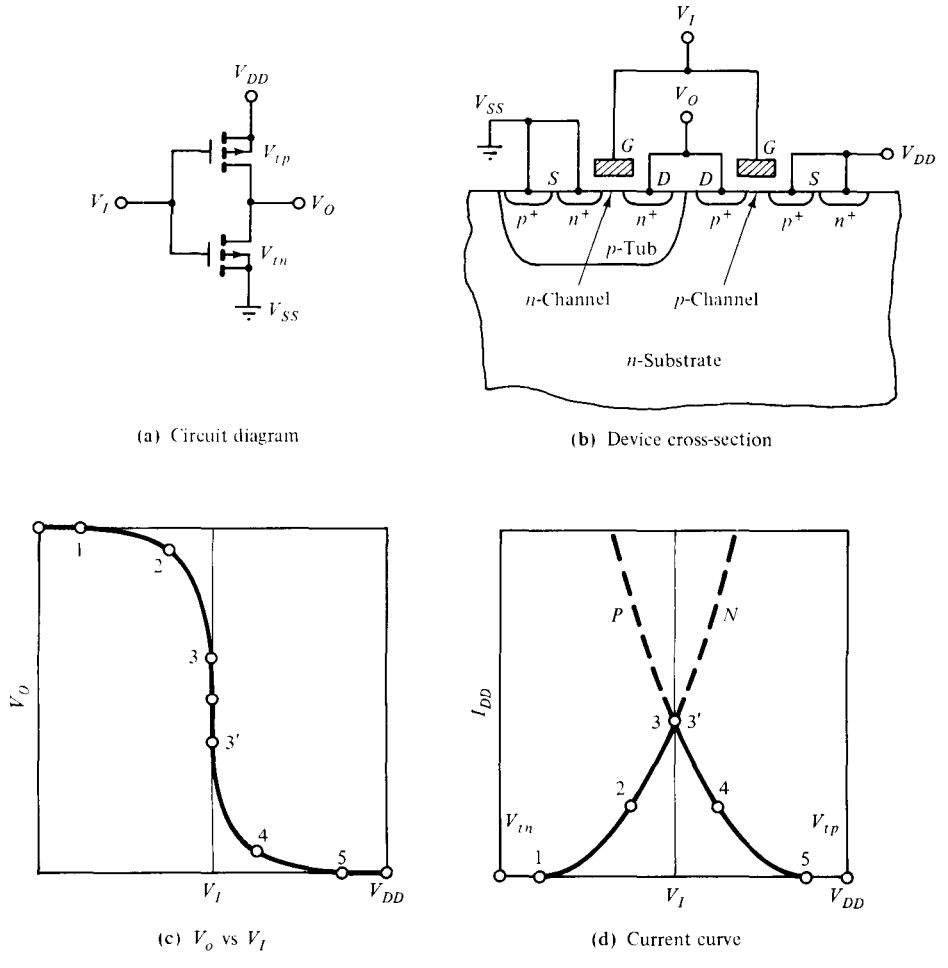


Figure 6-5-7 CMOS operation. (*After Parrillo [13]; reprinted by permission of the Bell Laboratory.*)

ON, while the p-channel transistor finally turns OFF. When $V_I > (V_{DD} - |V_{tp}|)$, the output voltage is $V_o = V_{SS}$.

The key feature of a CMOS gate is that in either logic state ($V_o = V_{DD}$ or V_{SS}) one of the two transistors is OFF and the current conducted between V_{DD} and V_{SS} is negligible. Figure 6-5-7(d) shows the current I_{DD} as a function of V_I. A significant current is conducted through the CMOS circuit only when both transistors are ON at the same switching time. The low power consumption of CMOS is one of its most important contributions. The performance and simplification of circuit design are other attractive features of the CMOS device. CMOS provide the circuit designer with flexibility in designing circuits that are either static CMOS (a p-channel transistor for every n-channel transistor) or dynamic CMOS (unequal number of n- and p-channel transistors).

6-5-3 Memory Devices

Memories are devices that can store digital data or information in terms of bits (binary digits). Many memory chips were designed and developed by using NMOS devices. The major semiconductor memory categories are ROM, PROM, EPROM, EEPROM, SRAM, BSRAM, and DRAM. The unit cells of the memory types are shown in circuit schematics in Fig. 6-5-8 [14].

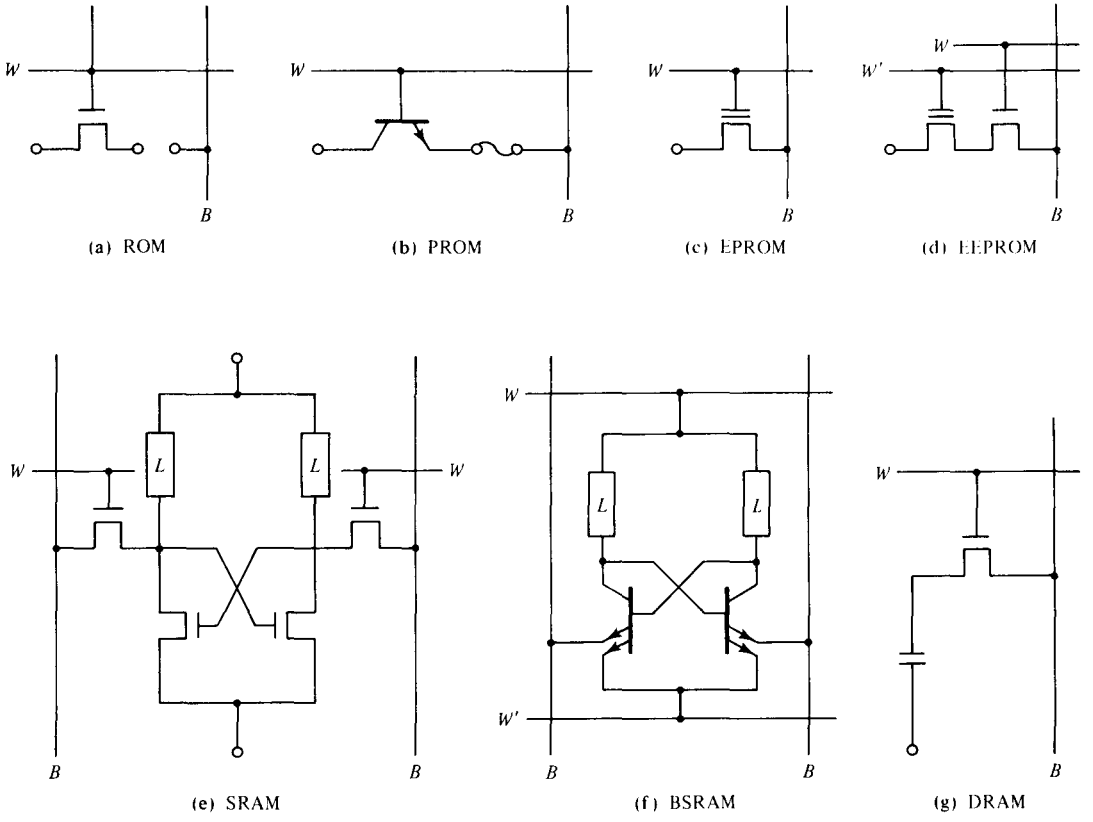


Figure 6-5-8 Circuit diagrams of memory types. (*After S. Asai [14]; reprinted by permission of IEEE, Inc.*)

ROM. The *read-only memory* (ROM) is also called *mask ROM*. During fabrication stage, the information is inscribed (and cannot be altered) in the form of presence or absence of a link between the word (access) line and the bit (sense) line. This causes the presence or absence of a readout signal on the bit line when the word line is activated. The essential part of the ROM is the way the link is provided, since the link determines the cell size (and thus the cost per bit) and the turnaround time (TAT). Fast, high-density ROMs are in great demand for personal computers.

PROM. The *programmable read-only memory* (PROM) is one of the ROMs that are field-programmable but lack "erase" capability. PROM uses cells with a fuse that can be blown open electrically, or a p-n diode that can be short-circuited by an avalanching pulse. A bipolar PROM has 64-Kbit p-n diode cells, and MOS PROMs have higher density but slower speed.

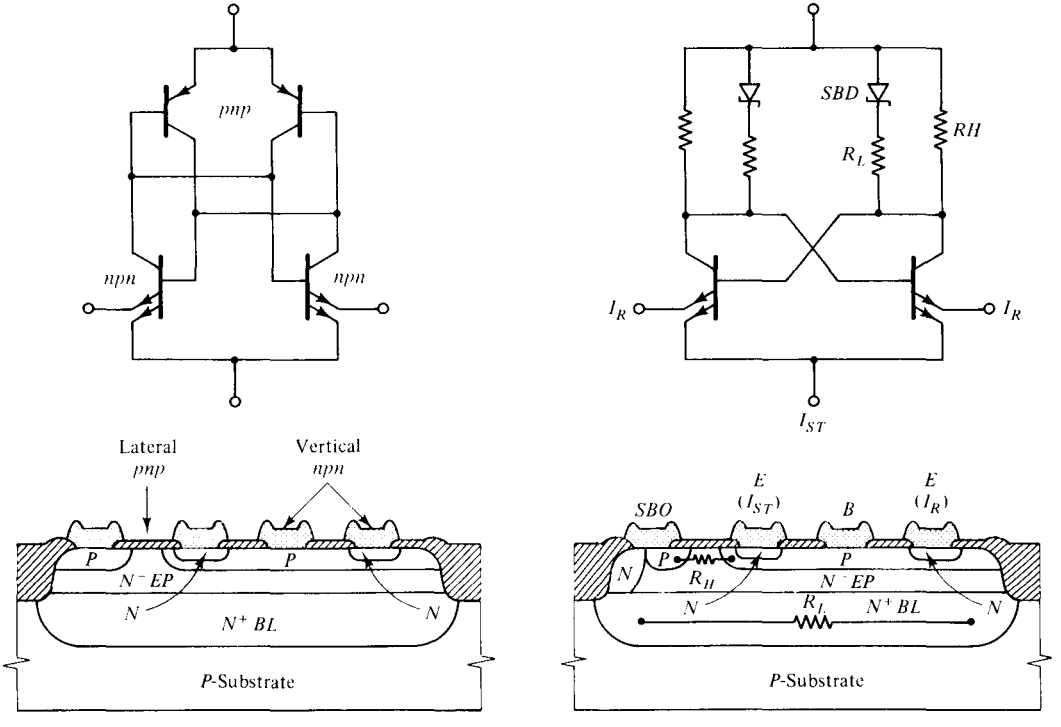
EPROM. EPROM stands for the *erasable programmable read-only memory*. In the EPROM cell, the presence or absence of charge in the floating gate of a double-poly-gate MOSFET determines the logic state. Programming is done by injecting energetic carriers generated by drain p-n junction avalanche breakdown, thereby increasing the threshold voltage V_{th} of the memory transistor. The EPROM is, therefore, also called the FAMOS (*floating-gate avalanche injection MOS*) device. When ultraviolet light is shone on the device, the charge in the floating gate is released, thereby erasing the memory. EPROMs are therefore packaged with a glass window to permit the erasing operation to occur. The original p-channel FAMOS cell, which has two transistors in series—one for storage and the other for access, has been replaced by n-channel, single-transistor cells. The original programming voltage of 30 V has been reduced to around 12 V. The most advanced 1-Mbit EPROMs today have a cell size of 19–29 μm^2 and an access time of 80–140 ns.

EEPROM. EEPROM designates the *electrically erasable programmable read-only memory*, and it is the most sophisticated in its principle of operation. For a ROM to be electrically erasable, it must have the means to inject and extract charge carriers into and from a floating gate. The first proposal for an EEPROM used the electron-trapping states at the nitride-oxide interface in a metal-nitride-oxide-silicon (MNOS) structure with a very thin (about 2 nm) oxide. The recent dominant technology of EEPROM uses a floating gate separated from the silicon by an oxide (about 150Å thick). Programming and erasing in either type of EEPROM is achieved by forcing the channel current to flow between the gate and substrate with the control biased and negative, respectively.

Both EPROM and EEPROM store charge on a conductive region in the middle of a MOS-gate oxide, and are, therefore, critically dependent on MOS structure, especially high-field carrier transport in both silicon and oxide. Because carriers in the floating island stay there even after the power supply is turned off, EPROM and EEPROM are also nonvolatile memories.

SRAM. The *random-access memory* (RAM) is one of the largest memories. In a RAM, memory cells are organized in a matrix form, and they can be accessed in random order to read (retrieve) or write (store) data. A *static random-access memory* (SRAM) can retain stored data indefinitely, and it can be implemented as a flip-flop circuit to store one bit of information. Since SRAMs use flip-flop ciruits in the memory cells, they are the most basic of all semiconductor memories. Active devices for access and drive are either MOS transistors or bipolar transistors.

BSRAM. The *bipolar SRAM* (BSRAM) is the fastest of all the semiconductor memory types, but MOS SRAM is the fastest among MOS memories. Figure 6-5-9 shows the equivalent-circuit diagrams for bipolar SRAMs.



(a) Cross-coupled *p-n-p* load cell (b) Equivalent circuit for bipolar SRAM

Figure 6-5-9 Circuit diagram for BSRAM.

DRAM. The first *dynamic random-access memory* (DRAM) used one-half of the static memory cell, or three transistors—one for the driver, another for the load, and the third for the access. This device has evolved to today's one-transistor, one-capacitor DRAM cell, in which the single transistor is used as the access to the capacitive reservoir. Since the stored charge is gradually lost because of the space-charge generation-recombination process, cells have to be read and refleshed at predetermined intervals on the order of milliseconds (hence, the name *dynamic*). The DRAM readout signal is small, on the order of 150–200 mV, and is subject to various kinds of noise sources.

6-6 CHARGE-COUPLED DEVICES (CCDs)

The *charge-coupled device* (CCD) is a metal-oxide-semiconductor (MOS) diode structure that was proposed in 1969 by Boyle and Smith [15, 16]. The CCD can move the charges in the MOS diode along a predetermined path under the control of

clock pulses, and so it is also called the charge-transfer device (CTD). CCDs have many microwave applications, such as in infrared detection and imaging and digital signal processing. There are three basic types of CCDs: surface-channel CCD (SCCD), buried-channel CCD (BCCD), and junction CCD (JCCD). In the SCCD or BCCD the charge is stored and transferred at the semiconductor surface or in the semiconductor interior, respectively; whereas in the JCCD the store and transfer of the charge packet occur at the p-n junction.

The motion of the charge packets in a charge-coupled device is transversely controlled by the applied gate voltages. This phenomenon is similar to the carrier motion in a microwave field-effect transistor like MESFET or MOSFET. In effect, the CCD can be referred to as the field-effect CCD.

6-6-1 Operational Mechanism

A charge-coupled device (CCD) is an array of many MOS or MIS diodes. In operation, the information (or signal) is stored in the form of electrical charge packets in the potential wells created in a MOS diode. Under the control of externally applied voltage (i.e., gate voltage), the potential wells and the charge packets can be shifted from one well to an adjacent one rapidly through the entire CCD structure.

Three separate mechanisms allow the charge packets to move from one well to another: self-induced drift, thermal diffusion, and fringing field drift. Thermal diffusion results in an exponential decay of the remaining charge under the transferring electrode. The fringing field is the electric field in the direction of charge flow and it can help speed the charge-transfer process considerably. Self-induced drift (or a charge-repulsion effect) is only important at relatively large signal-charge densities. It is the dominant mechanism in the transfer of the first 99% of the charge signal.

Energy band of MIS diode. A single MIS structure on an n-type semiconductor (or p-type semiconductor) is the basic element of the CCD. Figure 6-6-1 shows the energy band diagrams for a MIS structure [15].

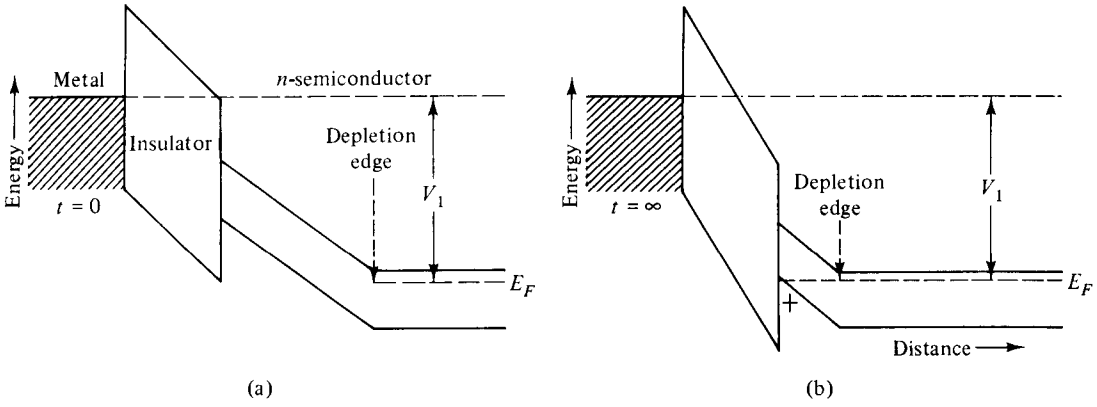


Figure 6-6-1 Energy-band diagrams of MIS structure. (*From W. S. Boyle and G. E. Smith [15]; reprinted with permission from The Bell System, AT&T.*)

The voltage applied to the metal electrode is negative with respect to the semiconductor and large enough to cause depletion. When the voltage is first applied at $t = 0$, there are no holes at the insulator-semiconductor interface [see Fig. 6-6-1(a)]. As holes are introduced into the depletion region, they will accumulate at the interface and cause the surface potential to be more positive [see Fig. 6-6-1(b)].

Three-phase structure. The CCD can be constructed in the form of a typical three-phase structure as shown in Fig. 6-6-2 [16].

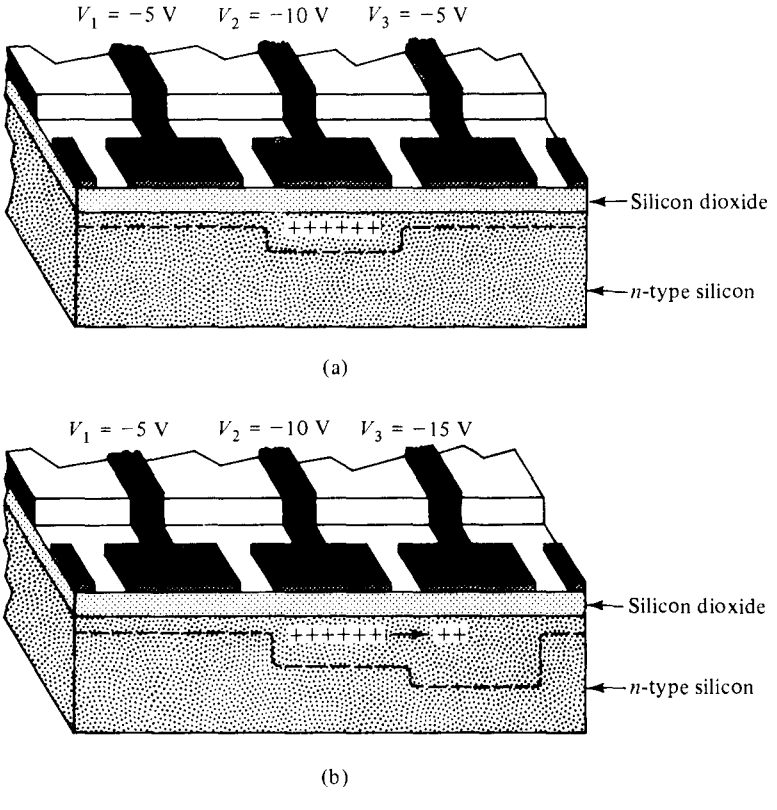


Figure 6-6-2 Cutaway of CCD. (*From W. S. Boyle and G. E. Smith [16]; reprinted by permission of the IEEE, Inc.*)

The CCD consists of a closely spaced array of MIS diodes on an n-type semiconductor substrate with a large negative gate voltage applied. Its basic function is to store and transfer the charge packets from one potential well to an adjacent one. As shown in Fig. 6-6-2(a), $V_1 = V_3$ and V_2 is more negative. In effect, a potential well with stored holes is created at gate electrode 2. The stored charge is temporary because a thermal effect will diffuse the holes out of the wells. Therefore the switching time of the voltage clock must be fast enough to move all charges out of the occupied well to the next empty one. When the voltage V_3 is pulsed to be more negative than the other two voltages V_1 and V_2, the charge begins to transfer to the potential well at gate electrode 3 as shown in Fig. 6-6-2(b).

Store and transfer of charge packets. A linear array of MIS diodes on an n-type semiconductor is shown in Fig. 6-6-3 [15].

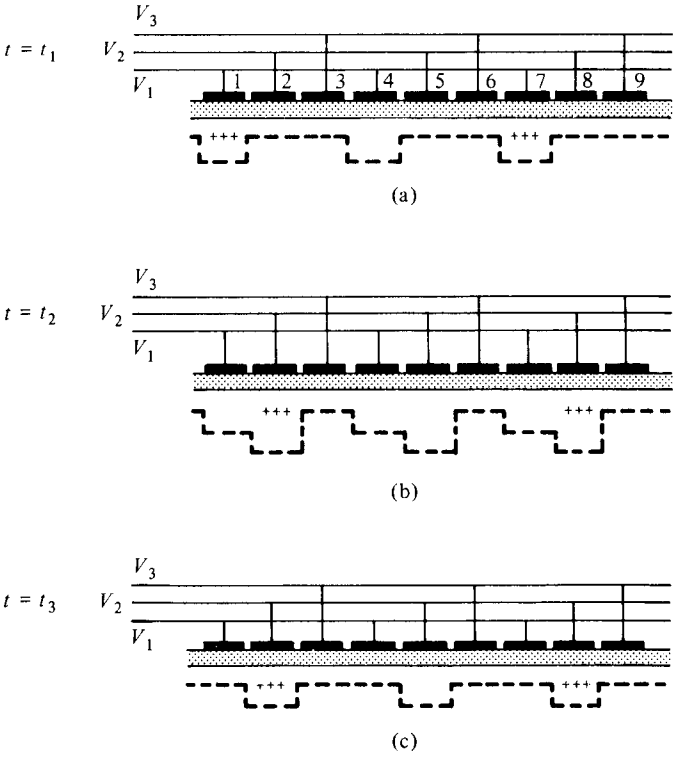


Figure 6-6-3 Store and transfer of charge packets for a three-phase CCD. (*From W. S. Boyle and G. E. Smith [15]; reprinted by permission of The Bell System, AT&T.*)

For a three-phase CCD, every third gate electrode is connected to a common line (see Fig. 6-6-3). At $t = t_1$, a more negative voltage V_1 is applied to gate electrodes 1, 4, 7, and so on, and less negative voltages V_2 and V_3 ($V_2 = V_3$) are applied to the other gate electrodes. It is assumed that the semiconductor substrate is grounded and that the magnitude of V_1 is larger than the threshold voltage V_{th} for the production of inversion under steady-state conditions. As a result, positive charges are stored in the potential wells under electrodes 1, 4, 7, . . . as shown in Fig. 6-6-3(a).

At $t = t_2$, when voltage V_2 at gate electrodes 2, 5, 8, . . . is pulsed to be more negative than V_1 and V_3, the charge packets will be transferred from the potential wells at gate electrodes 1, 4, 7, . . . to the potential minimum under gate electrodes 2, 5, 8, . . . as shown in Fig. 6-6-3(b).

At $t = t_3$, when voltages $V_1 = V_3$ and voltage V_2 remains more negative, the charge packets have been transferred one spatial position and the sequence is ready to continue as shown in Fig. 6-6-3(c).

6-6-2 Surface-Channel Charge-Coupled Devices (SCCDs)

A surface-channel charge-coupled device (SCCD) is basically an MOS-diode structure as shown in Fig. 6-6-4(a) [28]. Its energy band diagrams are illustrated in parts (b) and (c).

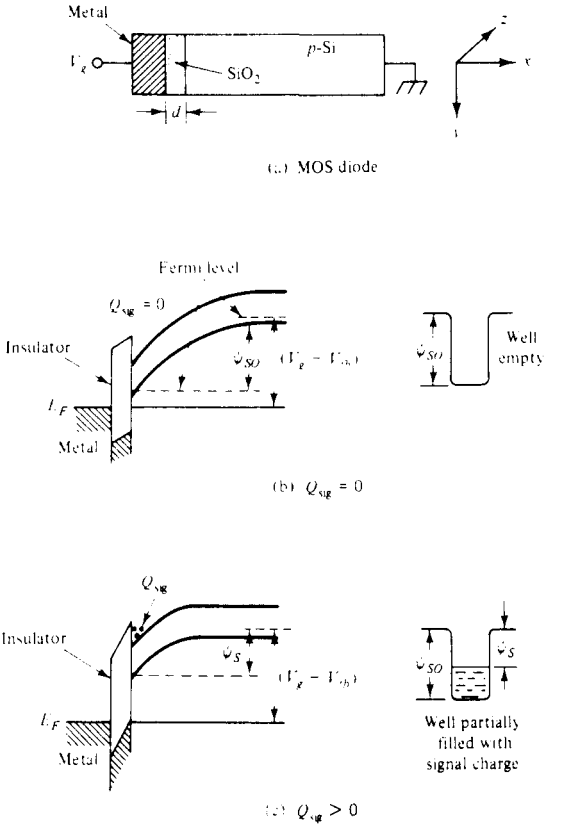


Figure 6-6-4 Physical structure and energy-band diagrams of a BCCD. (*From D. F. Barle [28]; reprinted with permission of the IEEE, Inc.*)

There are two cases for the creation of a charge packet under deep depletion.

1. Zero Signal-Charge ($Q_{sig} = 0$). When the signal charge is zero, an empty well is formed by the potential minimum at the semiconductor surface as shown in Fig. 6-6-4(b). Gate voltage V_g and surface potential ψ_s are related by

$$V_g - V_{fb} = V_i + \psi_s = \frac{qN_aW}{C_i} + \psi_s \tag{6-6-1}$$

where V_{fb} = flatband voltage
V_i = voltage across the insulator
$W = \left(\frac{2\epsilon_s \psi_s}{qN_a}\right)^{1/2}$ in the depletion width

Substitution of the depletion width into Eq. (6-6-1) yields

$$V_g - V_{fb} = \frac{1}{C_i}(2\epsilon_s q N_a \psi_s)^{1/2} + \psi_s \tag{6-6-2}$$

2. Stored Signal-Charge ($Q_{sig} > 0$). When a signal-charge packet is stored at the semiconductor surface, the surface potential decreases and the potential well is partially filled as shown in Fig. 6-6-4(c). The surface potential equation of Eq. (6-6-2) becomes

$$V_g - V_{fb} = \frac{Q_{sig}}{C_i} + \frac{1}{C_i}(2\epsilon_s q N_a \psi_s)^{1/2} + \psi_s \tag{6-6-3}$$

The maximum charge density (electron or hole) that can be stored on an MOS capacitor is approximately equal to

$$N_{max} \simeq \frac{C_i V_g}{q} \qquad \text{for } V_g \gg 1 \tag{6-6-4}$$

6-6-3 Dynamic Characteristics

The dynamic characteristics can be described in terms of charge-transfer efficiency η, frequency response, and power dissipation.

Charge-transfer efficiency η. The charge-transfer efficiency is defined as the fraction of charge transferred from one well to the next in a CCD. The fraction left behind is the transfer loss and it is denoted by ϵ. Therefore the charge-transfer efficiency is given by

$$\eta = 1 - \epsilon \tag{6-6-5}$$

If a single charge pulse with an initial amplitude P_0 transfers down a CCD register, after n transfers, the amplitude P_n becomes

$$P_n = P_0 \eta^n = P_0(1 - n\epsilon) \qquad \text{for } \epsilon \ll 1 \tag{6-6-6}$$

where n equals the number of transfers or phases.

If many transfers are required, the transfer loss ϵ must be very small. For example, if a transfer efficiency of 99.99% is required for a three-phase, 330-stage shift register, the transfer loss must be less than 0.01%. The maximum achievable transfer efficiency depends on two factors: how fast the free charge can be transferred between adjacent gates and how much of the charge gets trapped at each gate location by stationary states.

Frequency response. There are, in fact, upper and lower frequency limitations for CCDs. The potential well will not remain indefinitely, and thermally generated electrons (or holes) eventually fill the well completely. Also, the time stored by the charge must be much shorter than the thermal relaxation time of the CCD's capacitor. So the maximum frequency is limited by the channel length L.

Power dissipation. The power dissipation per bit is given by

$$P = nfVQ_{\max} \tag{6-6-7}$$

Example 6-6-1: Power Dissipation of a Three-Phase CCD

A three-phase CCD is operating under the following conditions:

Applied voltage:	$V = 10$ volts
Number of phases:	$n = 3$
Maximum stored charges:	$Q_{\max} = 0.04$ pC
Clock frequency:	$f = 10$ MHz

Determine the power dissipation per bit.

Solution From Eq. (6-6-7) the power dissipation per bit is

$$P = nfVQ_{\max} = 3 \times 10^7 \times 10 \times 0.04 \times 10^{-12}$$
$$= 12\ \mu W$$

Charge-coupled devices (CCDs) have many microwave applications in electronic components and systems, such as in infrared systems and signal processing.

Infrared detection and imaging. Because varying amounts of charge corresponding to information can be introduced into the potential wells at one end of the CCD structure to emerge after some delay at the other end, the CCD is capable of detecting and imaging the infrared light from a target [17]. Ten years ago, when the CCD was first developed, only an array of 12 × 12 photodetectors could be used to detect the infrared images of a target. Because of the availability of greatly improved CCDs, today an array of photodetectors, such as Indium Antimonide (InSb) 128 × 128, are used to form charge packets that are proportional to the light intensity of a target; and these packets are shifted to a detector point for detection, readout, multiplexing, and time delay and integration (TDI). In scanned IR systems TDI is one of the most important functions performed by CCDs. In such a system the scene is mechanically scanned across an array of detector elements. By using CCD columns to shift the detector output signals (in the form of charge packets) along the focal plane with the same speed as the mechanical scan moves the scene across the array, the signal-to-noise ratio can be improved by the square root of the number of detector elements in the TDI column.

Signal processing. The CCD can perform several analog and digital signal processing functions, such as delay, multiplexing, demultiplexing, transversal

filtering, recursive filtering, integration, analog memory, digital memory, and digital logic. Thus CCDs are being used widely in special applications for the very large scale integration (VLSI) circuits.

Example 6-6-2: Design of an *N*-Type Three-Phase Surface-Channel CCD

The n-type three-phase surface-channel CCD has the following specifications:

Electron density:	$N_{max} = 2 \times 10^{12}\ \text{cm}^{-2}$
Insulator relative dielectric constant:	$\epsilon_{ir} = 3.9$
Insulator thickness:	$d = 0.15\ \mu\text{m}$
Insulator cross section:	$A = 0.5 \times 10^{-4}\ \text{cm}^2$
Power dissipation allowable per bit:	$P = 0.67\ \text{mW}$

a. Compute the insulator capacitance in farads per square centimeter.
b. Determine the maximum stored charges per well in coulombs.
c. Find the required applied gate voltage in volts.
d. Choose the clock frequency in megahertz.

Solution

a. The insulator capacitance is

$$C_i = \frac{\epsilon_i}{d} = \frac{3.9 \times 8.854 \times 10^{-12}}{0.15 \times 10^{-6}} = 23\ \text{nF/cm}^2$$

b. The maximum stored charges per well is

$$Q_{max} = N_{max} qA = 2 \times 10^{12} \times 1.6 \times 10^{-19} \times 0.5 \times 10^{-4}$$
$$= 16\ \text{pC}$$

c. From Eq. (6-6-4) the required applied gate voltage is

$$V_g = \frac{N_{max} q}{C_i} = \frac{2 \times 10^{12} \times 1.6 \times 10^{-19}}{23 \times 10^{-9}} = 14\ \text{V}$$

d. From Eq. (6-6-7) the clock frequency is

$$f = \frac{P}{nVQ_{max}} = \frac{0.67 \times 10^{-3}}{3 \times 14 \times 16 \times 10^{-12}} = 1\ \text{MHz}$$

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PROBLEMS

JFETs

6-1. A silicon JFET has a gate length of 5 μm. Calculate the maximum frequency of oscillation for the device.

6-2. An n-channel silicon JFET has the following parameters:

Electron density:	$N_d = 2 \times 10^{17}$ cm^{-3}
Channel height:	$a = 0.4 \times 10^{-4}$ cm
Relative dielectric constant:	$\epsilon_r = 11.8$

Compute the pinch-off voltage.

6-3. An n-channel silicon JFET at 300° K has the following parameters:

Electron density:	$N_d = 5 \times 10^{17}$ cm^{-3}
Hole density:	$N_a = 8 \times 10^{18}$ cm^{-3}
Dielectric constant:	$\epsilon_r = 11.8$
Channel height:	$a = 0.3 \times 10^{-4}$ cm
Channel length:	$L = 6 \times 10^{-4}$ cm
Channel width:	$Z = 45 \times 10^{-4}$ cm
Electron mobility:	$\mu_n = 520$ cm^2/V·s
Drain voltage:	$V_d = 8$ V
Gate voltage:	$V_g = -1$ V

Compute:

a. The pinch-off voltage in volts
b. The pinch-off current in mA
c. The built-in voltage in V
d. The drain current in mA
e. The saturation drain current at $V_g = -1$ V in mA
f. The cut-off frequency in GHz

6-4. An n-channel silicon JFET at 300° K has the following parameters:

Electron density:	$N_d = 3 \times 10^{17}$ cm^{-3}
Hole density:	$N_a = 2 \times 10^{19}$ cm^{-3}
Relative dielectric constant:	$\epsilon_r = 11.8$
Channel height:	$a = 0.5 \times 10^{-4}$ cm
Channel length:	$L = 10 \times 10^{-4}$ cm
Channel width:	$Z = 20 \times 10^{-4}$ cm
Drain voltage:	$V_d = 7$ V
Gate voltage:	$V_g = -1.5$ V

Determine:

a. The electron mobility μ_n
b. The pinch-off voltage in V
c. The pinch-off current in mA
d. The drain current in mA
e. The saturation current in mA at $V_g = 0$
f. The cutoff frequency in GHz

6-5. Verify Eq. (6-1-17) from Eq. (6-1-12).

6-6. Write a FORTRAN program to compute the drain current of an n-channel silicon JFET. The device parameters are as follows:

Electron concentration:	$N_d = 2 \times 10^{23}$ m^{-3}
Channel height:	$a = 0.2 \times 10^{-6}$ m
Relative dielectric constant:	$\epsilon_r = 11.8$
Channel length:	$L = 10 \times 10^{-6}$ m
Channel width:	$Z = 60 \times 10^{-6}$ m
Drain voltage:	$V_d = 0$ to 6 V
Gate voltage:	$V_g = 0$ to -3 V
Saturation drift velocity:	$v_s = 10^5$ m/s

The program specifications are

1. The drain voltage V_d varies from 0 to 6 volts with an increment of 1 volt per step
2. The gate voltage V_g varies from 0 to -3 volts with a decrease of -0.5 volt per step
3. The electron mobility μ varies from 0.9 to 0.3 m^2/V·s with a decrease of 0.1 per step
4. Use F10.5 format for numerical outputs and Hollerith format for character outputs
5. Print the outputs in three columns for drain voltage V_d (volts), gate voltage V_g (volts), and drain current I_d (mA)

MESFETs

6-7. A MESFET has a gate width of 5 μm. Calculate the maximum frequency of oscillation for the device.

6-8. A GaAs has a thickness of 0.40 μm and a doping concentration N_d of 5×10^{17} cm^{-3}. The relative dielectric constant ϵ_r of GaAs is 13.10. Calculate the pinch-off voltage in volts.

6-9. An n-channel GaAs MESFET at 300° K has the following parameters:

Donor density:	$N_d = 2 \times 10^{17}$ cm^{-3}
Relative dielectric constant:	$\epsilon_r = 13.10$
Channel height:	$a = 0.3 \times 10^{-4}$ cm
Channel length:	$L = 10 \times 10^{-4}$ cm
Channel width:	$Z = 50 \times 10^{-4}$ cm
Drain voltage:	$V_d = 7$ V
Gate voltage:	$V_g = -1.5$ V
Saturation drift velocity:	$v_s = 10^{-7}$ cm/s

Compute:

a. The electron mobility (read from Fig. A-2 in Appendix A)
b. The pinch-off voltage in V
c. The saturation current at $V_g = 0$
d. The drain current I_d in mA

6-10. An n-channel GaAs MESFET at 300° K has the following parameters:

Donor density:	$N_d = 3 \times 10^{17}$ cm^{-3}
Relative dielectric constant:	$\epsilon_r = 13.10$
Channel height:	$a = 0.5 \times 10^{-4}$ cm
Channel length:	$L = 8 \times 10^{-4}$ cm
Channel width:	$Z = 60 \times 10^{-4}$ cm
Drain voltage:	$V_d = 6$ V
Gate voltage:	$V_g = -2.0$ V
Saturation drift velocity:	$v_s = 1 \times 10^{7}$ cm/s

Calculate:

a. The electron mobility (read from Fig. A-2 in Appendix A)
b. The pinch-off voltage
c. The saturation current at $V_g = 0$
d. The drain current I_d in mA

6-11. A certain n-channel GaAs MESFET has the following parameters:

Electron concentration:	$N = 2.38 \times 10^{23}$ m^{-3}
Channel height:	$a = 0.2$ μm
Relative dielectric constant:	$\epsilon_r = 13.10$
Channel length:	$L = 10$ μm
Channel width:	$Z = 60$ μm
Electron mobility:	$\mu = 0.3$ m^2/V · s
Drain voltage:	$V_{ds} = 6$ volts
Gate voltage:	$V_g = -3$ volts
Saturation drift velocity:	$v_s = 10^5$ m/s

a. Calculate the pinch-off voltage.
b. Compute the velocity ratio.
c. Determine the saturation drain current at $V_g = 0$.
d. Find the drain current I_d.

HEMTs

6-12. Describe the structure of a HEMT and its fabrication processes.

6-13. Describe the operating principles of a HEMT.

6-14. A HEMT has the following parameters:

Gate width:	$W = 140$ m
Electron velocity:	$v(z) = 3 \times 10^5$ m/s
2-D electron-gas density:	$n(z) = 6 \times 10^{15}$ m^{-2}

Compute the drain current of the HEMT.

6-15. A HEMT has the following parameters:

Gate width:	$W = 100$ m
Electron velocity:	$v(z) = 4 \times 10^5$ m/s
2-D electron-gas density:	$n(z) = 4 \times 10^{15}$ m^{-2}

Calculate the drain current of the HEMT.

6-16. A HEMT has the following parameters:

Threshold voltage:	$V_{th} = 0.15$ V
Donor concentration:	$N_d = 3 \times 10^{24}$ m^{-3}
Metal-semiconductor Schottky barrier potential:	$\psi_{ms} = 0.8$ V
AlGaAs dielectric constant:	$\epsilon_r = 4.43$

Compute:
a. The conduction–band-edge difference between GaAs and AlGaAs
b. The sensitivity of the HEMT

6-17. A HEMT has the following parameters:

Threshold voltage:	$V_{th} = 0.12$ V
Donor concentration:	$N_d = 5 \times 10^{24}$ m^{-3}
AlGaAs dielectric constant:	$\epsilon_r = 4.43$
Metal-semiconductor Schottky barrier potential:	$\psi_{ms} = 0.8$

Calculate:
a. The conduction–band-edge difference between GaAs and AlGaAs
b. The sensitivity of the HEMT

6-18. Describe the applications of a HEMT.

MOSFETs

6-19. A basic MOSFET is formed of Al metal, SiO_2 insulator, and Si semiconductor. The insulator capacitance is 4 pF and the channel length L is 12 μm.

a. Determine the drain current $I_{d\ sat}$ in the saturation region with $V_{th} = 2V$ and $V_{gs} = 4V$ for the enhancement mode.

b. Compute the transconductance g_m for the same mode.

c. Calculate the drain current $I_{d\ sat}$ in the saturation region with $V_{th} = -1.5V$ and $V_{gs} = 0V$ for the depletion mode.

d. Find the transconductance g_m for the depletion mode.

6-20. An Al-Oxide-Si MOSFET has an insulator capacitance of 3 pF and a channel length L of 10 μm. The gate voltage V_{gs} is 10 V and the threshold voltage is 1.5 V.

a. Determine the carrier drift velocity in real case.

b. Calculate the drain current.

c. Compute the carrier transit time.

d. Find the maximum operating frequency in GHz.

6-21. The insulator SiO_2 in a Si MOSFET has a relative dielectric constant ϵ_{ir} of 11.8 and a depth d of 0.08 μm. The channel length L is 15 μm and the channel depth Z is 150 μm. Calculate the insulator capacitance C_{in}.

6-22. Compare the advantages and disadvantages of a GaAs MOSFET with those of a Si MOSFET.

6-23. A certain p-channel MOSFET has the following parameters:

Doping concentration:	$N_a = 2 \times 10^{17}\ cm^{-3}$
Relative dielectric constant:	$\epsilon_r = 11.8$
Insulator relative dielectric constant:	$\epsilon_{ir} = 4$
Insulator thickness:	$d = 0.01\ \mu m$
Operating temperature:	$T = 320°\ K$

a. Calculate the surface potential ψ_s(inv) for strong inversion.

b. Compute the insulator capacitance.

c. Determine the threshold voltage.

6-24. A certain n-channel MOSFET has the following parameters:

Channel length:	$L = 5\ \mu m$
Channel depth:	$Z = 10\ \mu m$
Insulator thickness:	$d = 0.02\ \mu m$
Gate voltage:	$V_g = 8\ V$
Threshold voltage:	$V_{th} = 1.5\ V$
Electron velocity:	$v_s = 2 \times 10^7\ cm/s$
Insulator relative dielectric constant:	$\epsilon_r = 4$

a. Compute the insulator capacitance in mF/m^2.

b. Calculate the saturation drain current in mA.

c. Determine the saturation transconductance in millimhos.
d. Estimate the maximum saturation operating frequency in GHz.

NMOS, CMOS, and Memory Devices

6-25. Describe the structures of NMOS, PMOS, and CMOS devices.
6-26. Explain the operational principles of the NMOS, PMOS, and CMOS devices.
6-27. Discuss the logic-gate operations of NMOS, PMOS, and CMOS.
6-28. Describe the major memory devices.

CCDs

6-29. A charge-coupled device has 484 (or 22 × 22 array) elements each with a transfer inefficiency of 10^{-4} and is clocked at a frequency of 100 KHz.
a. Determine the delay time between input and output.
b. Find the percentage of input charge appearing at the output terminal.

6-30. A surface-channel CCD is operated by a gate voltage V_g of 10 volts. The insulator has a relative dielectric constant ϵ_r of 6 and a depth d of 0.1 μm. Determine the stored charge density on this MOS capacitor.

6-31. A p-type surface-channel CCD (Al-Oxide-Si) has the following parameters:

$$N_a = 10^{14}\ \text{cm}^{-3} \qquad Q_{in} = 10^{-8}\ \text{C/cm}^2$$
$$\phi_{ms} = -0.85\ \text{eV} \qquad \text{W} = 1\ \mu\text{m}$$
$$\epsilon_{ir} = 4 \qquad d = 0.1\ \mu\text{m}$$

a. Determine the flat-band potential.
b. Calculate the voltage across the insulator.

6-32. A three-phase CCD has $Q_{max} = 0.06$ pC operating at a clock frequency of 20 MHz with 10 volts applied. Determine the power dissipation per bit.

6-33. A three-phase JCCD has a length L of 8 μm, an electric field E_x of 480 V/cm, and an electron mobility μ_n of 1000 $\text{cm}^2/\text{V} \cdot \text{s}$. Calculate the signal carrier transit time.

6-34. An n-type three-phase SCCD has the following parameters:

Insulator relative dielectric constant:	$\epsilon_{ir} = 4$
Insulator thickness:	$d = 0.3\ \mu\text{m}$
Insulator cross section:	$A = 0.6 \times 10^{-4}\ \text{cm}^2$
Electron density:	$N_{max} = 4 \times 10^{12}\ \text{cm}^{-2}$
Power dissipation allowable per bit:	$P = 0.8\ \text{mW}$

a. Compute the insulator capacitance in F/cm^2.
b. Calculate the maximum stored charges per well in coulombs.
c. Find the required applied gate voltage in volts.
d. Choose the clock frequency in MHz.